SYNTHESIS AND SIMULATION OF NOVEL MULTI VALUED LOGIC PROCESSOR ARCHITECTURE

A Thesis
submitted in partial fulfillment of requirement
for the award of the degree of

DOCTOR OF PHILOSOPHY

In

ELECTRONICS AND TELECOMMUNICATION ENGINEERING

By

SATISH SUDHAKAR NARKHEDE
[Ref. No. PGS/1194]

Under guidance of

Dr. Bharat S. Chaudhari
Guide

Dr. Gajanan K. Kharate
Co-Guide

Department of Electronics and Telecommunication Engineering
Matoshri College of Engineering and Research Centre, Nasik

FEBRUARY 2016

CERTIFICATE

This is to certify that the thesis entitled **"SYNTHESIS AND SIMULATION OF NOVEL MULTI VALUED LOGICPROCESSOR ARCHITECTURE"**, being submitted by **Satish Sudhakar Narkhede** in partial fulfillment of requirement for the award of degree of **Doctor of Philosophy** in Electronics and Telecommunication Engineering at Savitribai Phule Pune University at Matoshri College of Engineering and Research Centre, Nasik is a bonafide record of the work carried out by him under my supervision and guidance. The results embodied in this thesis have not been submitted elsewhere in part or full for the award of any degree or diploma.

Prof. D. D. Dighe
Head, Dept of E&TC,
Matoshri College of
Engineering and
Research Center, Nasik

Dr. Gajanan K. Kharate
Co-Guide and Principal,
Matoshri College of
Engineering and Research
Center, Nasik

Dr. Bharat S. Chaudhari
Guide
Professor, Dept of E&TC,
Maharashtra Institute of Technology , Pune

CERTIFICATE OF THE GUIDE

It is certified that the work incorporated in the thesis, entitled **"SYNTHESIS AND SIMULATION OF NOVEL MULTI VALUED LOGIC PROCESSOR ARCHITECTURE"**, being submitted by **Satish Sudhakar Narkhede** was carried out by the candidate under our supervision and guidance. Such material as has been obtained from other sources has been duly acknowledged in the thesis.

Dr. Gajanan K. Kharate
Co-Guide
Principal,
Matoshri College of Engineering and Research Center, Nasik

Dr. Bharat S. Chaudhari
Guide
Professor, Dept of E&TC,
Maharashtra Institute of Technology , Pune

Date :

Place :

DECLARATION BY THE CANDIDATE

I declare that the thesis entitled ***"SYNTHESIS AND SIMULATION OF NOVEL MULTI VALUED LOGIC PROCESSOR ARCHITECTURE",*** submitted by me for the degree of **Doctor of Philosophy** is the record of work carried out by me during the period from February 2009 to February 2016 under the guidance of **Dr. Bharat S. Chaudhari** and **Dr. Gajanan K. Kharate** and has not formed the basis for the award of any degree, diploma, associate ship, fellowship, titles in any other University or other Institution of Higher learning.

I further declare that the material obtained by other sources has been duly acknowledged and credited in this thesis.

Date:

Place:

Mr. Satish Sudhakar Narkhede
Research Scholar
Matoshri College of Engineering and Research Center, Nasik

ACKNOWLEDGEMENT

I wish to express my first and foremost gratitude to my PhD guide Dr. Bharat S. Chaudhari and Dr. Gajanan K. Kharate without whom this study was inconceivable. I am indeed thankful to them for their valuable guidance and immense encouragement in carrying out this research.

I am thankful to Prof. D. D. Dighe, HoD, Dept. of E&TC, MCOE, Nasik, Dr. S. D. Pable Phd Coordinator, MCOE, Nasik for their support in this journey and to Dr. S.T. Gande, Principal, SITRC, Nasik for his comments and suggestions.

I sincerely appreciate valuable support and encouragement from Mr. R. S. Kothavale, Managing Trustee PICT, Pune, Mr. Swastik Sirsikar secretary PICT, Pune, Dr. P.T. Kulkarni, Principal, PICT, Pune and Dr. Yerram Ravinder, Head, Dept. of E&TC, PICT, Pune.

I am also thankful to Dr. M. V. Munot, Prof. L. P. Patil, Prof. S. S. Dudam, Dept of E&TC, PICT for their support and kind assistance in the execution of this project. I would also like to extend special thanks to my departmental and institutional colleagues at PICT.

I am greatly indebted to my parents, Late Mr. Sudhakar Narkhede and Late Mrs. Mandakini Narkhede for always be-showering their blessings and best wishes which has driven me so far and has been key to my success; today and always. I owe many thanks to my wife Dr. Kirti and son Tanay, who walked beside me, supported me along the way constantly, and encouraged me. I thank them for their patience, understanding, and love. They have been the lenders of their rights to my time.

I would like to extend my heartfelt thanks to one and all, who have helped me in this research and its successful completion.

Satish Sudhakar Narkhede

TABLE OF CONTENTS

ABSTRACT

Multi Valued Logic (MVL) is emerging as a thrust area of research due to several advantages offered by them over the conventional binary logic. The switching algebra has expanded from binary to penta level, progressing through ternary and quaternary levels and MVL has thereby experienced major evolution in the recent past. Ternary Logic, a logic with radix 3 i.e. 3 logic states, is a case of MVL and serves a promising alternative to the binary logic thus attracting a wide community of researchers to contribute in the design of ternary processor.Despite the potential advantages of ternary logic, realization of an efficient, realistic and a practical ternary processor is still a thrust area of research. This research aims to address some of these challenges and unidentified issues in the design of ternary processor.

With the recent technological advancements and the reported drawbacks of the CMOS level implementation, commercial realization of ternary circuits is watched with keen interest thereby motivating the wide community of researchers to explore the usability of various alternativesbeyond CMOS devices for implementing ternary circuits. This research presents a novel hybrid approach based on combination of MIFGMOS (Multi Input Floating Gate Metal Oxide Semiconductor) transistor and conventional MOSFET for the realization of the ternary gates. The basic and universal ternary gates are devised based on hybrid combination of devices. An extensive simulation of all the designed gates is carried out using TSPICE circuit simulator. The results demonstrate expected functionality of the devised hybrid gates and additionally signify improvement in the performance parameters. This research also extends the designed ternary gates to implement ternary combinational and

sequential circuits and finally realize the Ternary Arithmetic and Logic Unit. An extensive simulation of the TALU is carried out for 9 operations using TSPICE circuit simulator which demonstrates expected functionality and additionally signify good improvement in the performance parameters. A modified design of ternary decoder is designed that leads to reduction in circuit element count. A novel Ternary Level Shifter which has received meager attention in the reported literature is also implemented. The design of TLS exploits the controllability and tunability of the MIFGMOS transistor to obtain an intermediate voltage level and eliminates the need of passive components and an additional power supply. This research also identifies a functionality issue in the reported design of Ternary Full Adder and proposes a solution to the identified problem. The MIFGMOS transistor based hybrid approach for designing an efficient TALU, combines the virtues of both the devices and facilitates the significant reduction in the circuit element count of the ternary combinational circuits as compared to earlier reported methods.

The arithmetic and logical unit and the control unit are essentially the most important and the nerve centre of a processor. This research presents design and implementation of an efficient 4-trit Ternary ALU and Ternary Control Unit (TCU) for a ternary processor. The implementation of sub-program overloading feature makes its design unique, flexible and portable for further extension. The functionality of the TCU is verified using fifty seven instructions belonging to various addressing modes. The control signals required for the execution of the instructions are identified and further modelled using a hardware description language.

The efficient ternary circuits designed and implemented in this research address some of the major challenges and achieve improvement in the parameters. The designed TALU and TCU signify encouraging results that pave the path for further developments in ternary processors.

List of Figures

List of Tables

ABBREVIATION

MVL	Multi Valued Logic
nMOS	N channel Metal Oxide Semiconductor
pMOS	p channel Metal Oxide Semiconductor
STI	Standard Ternary Inverter
PTI	Positive Ternary Inverter
NTI	Negative Ternary Inverter
FGMOS	Field Effect Metal Oxide Semiconductor
PDP	Power Delay Product
CMOS	Complementary Metal Oxide Semiconductor
MIFG	Multiple Input Field Effect Transistor
HDL	Hardware Descriptive Language
CNTFET	Carbon Nano Tube Field Effect Transistor
QDGFET	Quantum Dot Gate Field Effect Transistor
TFA	Ternary Full Adder
THA	Ternary Half Adder
THS	Ternary Half Subtractor
TFS	Ternary Full Subtractor
TM	Ternary Multiplier
TC	Ternary Comparator
TLS	Ternary Level Shifter
FIS	Fuzzy Inference System
TALU	Ternary Arithmetic Logic Unit
ANFIS	Artificial Neuro Fuzzy Inference System

Chapter 1

INTRODUCTION

1.1 Preamble

Traditionally, digital computations are performed on two-valued logic [1]. However, in 1964 *Alexander* has introduced the new technology, Multi Valued Logic (MVL), which can drastically change the concept of the technology [2]. It was expected that the technological advances would bring back the discussion on commercial realization of MVL circuits [3]. The 20thcentury however, brought a focus on ternary radix .The radix *3* number system is known as *Ternary Logic*. As the value of radix increases, the information carrying capacity of each connection also increases.Hence, MVL digital realization would be more appropriate than binary [4]. It offers numerous advantages over the binary logic in the design of the digital system [5]. In MVL many logical and arithmetic operations could be executed with higher speed and smaller number of computation stages [6]. This chapter includes brief Literature survey, Current research status, Motivation, Objectives and Scope of the Research Work and Organization of the Thesis.

1.2 Multi Valued Logic

In 1964, a new technology, MVL, was proposed which can drastically change the concept of the technology. An excellent review of the first developments of MVL and its application to electronics, including a few circuit implementations was presented by *Epstein et al*. [7].MVL has radix greater than 2, while conventional binary logic

computations are performed only on two-valued logic. However, the main drawbacks of the binary integrated circuits are the interconnection and pin-out problems, which result in restrictions, process control and decision support system are not efficiently implementable only with binary logic [8]. To overcome these problems, logic with more than two values, i.e. MVL is used that has the following advantages [1]

1. In MVL, each wire can transmit more MVL information than a binary element. As a result, the number of connection inside the chip can be reduced.
2. Since each MVL element can process more information than a binary element, the complexity of circuits may be decreased.
3. The ON- and OFF-chip connections can be reduced to help alleviate the pin-out difficulties that arise with increasingly larger chips.
4. The speed of serial information transmission will be faster since the transmitted information per unit time is increased.

Due to several advantages offered by them over the binary logic, over the past decades, MVL has experienced a phenomenal growth. Unlike the binary logic, in MVL systems there are more than two authorized logic levels. Let us consider an m-valued function F(X) with k variables, where $X = \{x_1, x_2, x_3, \ldots, x_k\}$ and each x_i can adopt values from $M = \{0, 1, 2, \ldots, m-1\}$. Therefore the function F(X) is a mapping $f : M^k \rightarrow M$ and consequently there are m^{m^k} different functions possible in the set f. The logical and arithmetic operations can be performed on more than two logic values. As a result, in MVL many logical and arithmetic operations could be executed with higher speed and smaller number of computation stages [6]. It has therefore been watched with keen interests to overcome the challenges of binary logic

and solve numerous problems more efficiently thus casting its applications in the field of fuzzy logic, machine learning, artificial intelligence, data mining, robotics, digital signal processing, digital control systems and image processing.[4, 6].

Widespread popularity of ternary circuits attracted many contributions from the researchers, taking the baton ahead. *P C Balla et al*. [9] proposed a MOS ternary-logic family, which is comprised of a set of inverters, NOR gates, and NAND gates. These gates are used to design basic ternary arithmetic and memory circuits.*Rozan et al*. [10] utilized, VHDL simulator, a hardware description language, as a potential tool for the simulation of MVL logic circuits and systems. The work demonstrates how VHDL can be used as a potential tool for the simulation of multi-valued digital circuits and systems. *Masahiro et al*. [4] presented a novel ternary fuzzy processor using the logic oriented neural networks. The simulation results are illustrated to show how a ternary fuzzy inference engine can be realized by taking into consideration of advantages of neural networks. *Dhande et al*. [11, 12] exploited the existing VHDL as a potential EDA tool for the simulation of MVL circuits and system by considering signal 'Z' as one of the state of MVL system along with signals '0' and '1'(0 being ground potential, Z intermediate state and 1 as +5V state). The VHDL modeling and simulation of T-Gates and 1-bit multiplier circuit is described and commented. *Sheng et al*. [1] designed novel ternary logic gates using Carbon Nano Tube (CNT) FETs (CNTFETs). A resistive-load CNTFET-based ternary logic design has been proposed to implement ternary logic based on CNTFET and compared with the existing resistive-load CNTFET logic gate designs. *Supriya et al*. [13] discuss logic circuit designs using the circuit model of three-state Quantum Dot Gate Field Effect Transistors (QDGFETs). QDGFETs produce one intermediate

state between the two normal stable ON and OFF states due to a change in the threshold voltage over this range. Chapter 2 details the survey of reported contributions and summarizes their advantages with important findings.

The research contributions focusing on the commercial realization of ternary circuits has grown by leaps and bounds and receives exceptional attention. In spite of the significant advancements, theories predict several disadvantages of MVL and the studies demonstrate challenges in the realization of the ternary circuits.

1.3 Current Status

Following are the major challenges, limitations and unidentified issues which are identified based on the literature survey in the development of ternary logic,

- Only a limited soft computation approaches are explored
- CMOS based approach is popularly used without addressing its major disadvantages
- Use of CNTFET based approach that combines use of ternary and binary gates for design of ternary combinational circuits without detailing the design of Binary CNTFET based gates
- Functionality issue in the design of QDGFET based Ternary full adder.
- Meager attention to design of Ternary Level Shifter (TLS)
- Meager attention to design of ternary sequential circuits
- Simulation tools and VHDL based modeling are not fully exploited to design flexible ternary circuits.

This research addresses some of these challenges and unidentified issues.

1.4 Motivation

The literature reports wide assortment of various methods used for the development of the ternary circuits. The soft computation approaches and simulation tools like VHDL only demonstrate the functionality of the devised circuits without considering the challenges from the realization perspective and may lack sufficiently detailed information of the device.

In the popular CMOS based approaches, the reported disadvantages of high static power, requirement of large off-chip resistors, need of multiple supply voltages, use of depletion-mode MOSFETs outweigh its advantages and make them unsuitable for the upcoming technologies [6]. As reported by *Plummer et al.* [14] the upcoming era will be dominated by beyond CMOS devices. Some of the popular beyond CMOS devices like, the CNTFET are successfully used for the ternary circuits but suffer from large circuit elements and face challenges due to misaligned and mis-positioned CNTs, high resistance CNT metal contact, chemical doping and fabrication issues [6]. The QDGFET based circuits [15] are designed considering 500mV and thus the noise margin is compromised. Moreover, the design TFA needs a careful examination to verify its operation for all the combinations of the input. The meager attention received for the design of TLS is an additional challenge in the development of ternary processor. The use of additional power supplies obviously leads to the power consumption issues related to the voltage divider circuit. Moreover, there are limitations of the voltage divider to act as precise reference. It is

necessary to address this issue and propose a TLS without an additional power supply.

The literature reports wide contributions in VHDL simulation based approaches and device level realizations of various ternary circuits. Despite the potential advantages of ternary logic over the binary, realization of an efficient, realistic and a practical ternary processor is still a thrust area of research. The encouraging results and the limitations in the state of art methods continue to draw attention of the research community and demand further researches to investigate the simulation based approaches and also explore the suitability of other beyond-CMOS devices for the implementation of ternary logic. This research aims to address some of these challenges and unidentified issues in the design of ternary processor.

1.5 Objectives and Scope of the Research Work

This research work is based on ternary logic. The ternary logic is a special case of MVL. The prime objective of this research work is to develop, simulate and test the ternary logic circuits and propose ternary logic processor architecture. This work includes the basic objectives:

1. To carry out an extensive survey of MVL.
2. To study and develop the algebra and calculus of ternary logic.
3. To study various switching devices that supports ternary logic system.
4. To Develop the combinational and sequential ternary logic circuits required to propose the ternary logic processor
5. To propose the basic architecture of ternary logic processor.
6. To simulate and test the basic modules of proposed architecture.

In this research work the modules are simulated using VHDL and performance is evaluated. Hardware implementation of the tested modules is beyond the scope of this research.

1.6 Organization of the Thesis

The thesis is comprised of six chapters. Chapter 1 includes an introduction, the basic terminologies of MVL, its various applications, current status, motivation, objectives and scope of the research work.

Chapter 2 describes the literature survey and review of the existing approaches in designing the ternary circuits. The challenges and the limitations of the existing switching technologies and approaches are highlighted.

Chapter 3 covers the research methodology for exploring the switching device, MIFGMOS in ternary prospects. Novel hybrid approaches for design of ternary combinational and sequential circuits for the ternary processor are presented.

Chapter 4 describes the design and simulation of extended modules for the functional verification of TCU and the ternary instruction set. Chapter 5 presents the results and discussions that detail the contributions of this research.

Chapter 6 comprises of the conclusions and the future scope. The author's research publications are included followed by the references used in this research.

Chapter 2

LITERATURE SURVEY

Traditionally, digital computations are performed on two-valued logic named as Binary Logic. The binary logic faces major challenges of the interconnections and pin-out problems when designing large and dense chips. This restricts the number of connections inside and outside of the circuits. . However, in 1964, a new technology, MVL, was proposed which can drastically change the concept of the technology.Epstein et al. summarizes the initial developments of MVL and highlights the major applications of MVL across the various domains [16]. MVL systems lead to saving in the number of interconnections. Due to the availability of the additional bits (logic levels), the wires convey more information. It ultimately reduces the number of pins and leads to their saving. The information stored per memory cell also increases with use of MVL. These advantages of MVL directly contribute to reduction in the memory and thus the hardware cost [17]. The significant advantages offered by MVL of reduced complexity in the design, smaller on chip area leading to increased density of fabrication and high-bandwidth parallel and serial data transfer make it an attractive and a thrust area of research [6]. Ternary logic is a specialized MVL that demonstrates use of three significant logic levels, true, false and intermediate.

This chapter presents a Theory of Ternary Logic and survey of the advancements in the ternary domain in terms of the design, realization / implementation and simulation of the ternary gates,

combinational and sequential circuits. The chapter also presents a brief survey of the expansion in the MIFG based designs and their usability for ternary logic. The chapter concludes detailing the challenges and issues in the reported literature.

2.1 Ternary Logic

The ternary logic or radix 3 number system, known as *Ternary Logic* is the special case of MVL with three logic levels. Ternary means a switching element, which switches among 3 states namely 0, 1 and 2 voltage states or true, intermediate and false. Many ternary logic models exist in the literature, but they generally involve high power consumption even in static state Customized technological processes [1] or multi-threshold devices [18], Current-mode MVL techniques also exist [9], but they are not feasible for present high performance applications as high-speed performance and low–power dissipation can be obtained using the CMOS technology.

Ternary logic offers several important advantages over the binary logic in the design of the digital system. More information can be transmitted over a given set of lines or stored for a given register length, the complexity of interconnections can be reduced, reduction in the chip area can be achieved and more efficient error detection and error correction code can be employed [9] using Ternary Logic. Additionally the memory requirement will be drastically reduced.

2.1.1 Ternary Logic Preliminaries

Due to the advantages offered by the Ternary Logic the domain is an area of the keen research.The researchers have proposed two different ternary logic systems such as balanced and unbalanced logic system. Balanced or symmetric system uses $-V_{DD}$ for logic 0, 0V for

logic 1 and $+V_{DD}$ for logic 2. An unbalanced or ordinary system uses 0V for logic 0, $V_{DD}/2$ for logic 1 and, V_{DD} for logic 2.

In ternary system, i.e. radix 3 system, the numbers of possible functions are 3^{3^3} leading to 19683 logical operations. Max, Min Literals, successor, inverter are few of them which will be detailed in the next section.

2.1.2 Ternary Algebra and Minimization Techniques

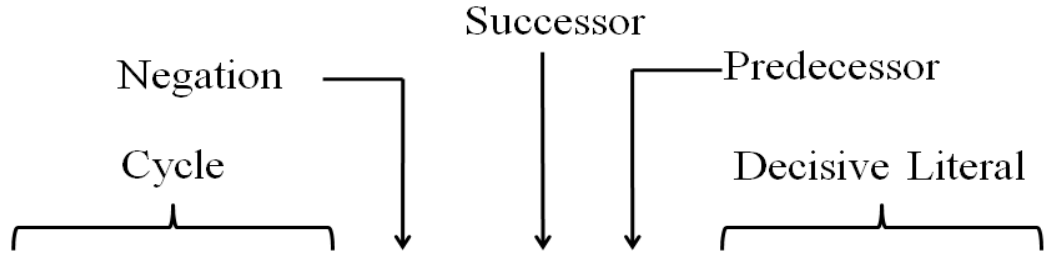
Ternary logic demands a functionally complete algebra in order to have the ability to describe all possible functions (19683 logical operations). Since Boolean algebra is not in general adequate for multiple-valued functions due to its lack of completeness over sets of logic values that do not have a cardinality of 2n, it is necessary to consider alternative algebraic structures.

One of the first published ternary logic systems in a modern form was due to the work of Lukasiewicz in Poland in 1920 [19]. This system was motivated by the consideration of a third logic value of *indeterminate* in addition to the values representing *true* and *false.* A variation of the ternary logic system of Lukasiewicz was developed by Bochvar 1939 [20]. The variation was due to a difference in the semantical interpretation of the third logic value. The *indeterminate* logic value as defined by Lukasiewicz was construed by Bochvar as an *undecidable* value. Although the MVL logic of Lukasiewicz was published one year earlier than the work of Emil Post in 1921 [21], the Post algebras are commonly cited as the first example of a MVL algebra since the “chained Post algebra” is functionally complete and that of Lukasiewicz was not. Another ternary logic system was proposed by Kleene in 1938 [22]. As is the case of the Bochvarianternary logic system, the difference in the Kleene system

can be considered to be a different interpretation of the third logic value.

Table 2.1 summarizes various unary operators for ternary logic and table 2.2 shows different operations on unary operators.

Table 2.1: Summarizes various unary operators for a ternary logic



X	X^1	X^2	$\overline{X}$	$\overrightarrow{X}$	$\overleftarrow{X}$	$C_0(X)$	$C_1(X)$	$C_2(X)$
0	1	2	2	1	2	2	0	0
1	2	0	1	2	0	0	2	0
2	0	1	0	0	1	0	0	2

Table 2.2: Two place operators like min, max and mod-sum that correspond to the familiar AND, OR, and EXOR functions

Min (x,y)

x, if $x < y$

y, otherwise

X \ Y	0	1	2
0	0	0	0
1	0	1	1
2	0	1	2

Max (x ,y)

x, if $x > y$

y, otherwise

X \ Y	0	1	2
0	0	1	1
1	1	1	2
2	2	2	2

Mod-sum

X \ Y	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

Mod-difference

X \ Y	0	1	2
0	0	2	1
1	1	0	2
2	2	1	2

While the system of Lukasiewicz contained the *indeterminate* value and the system of Bochvar an *undecidable* value, the third value in the Kleene system is interpreted as simply an *unknown* value. This interpretation is analogous to the *X* value used in the VHDL and Verilog HDLs for initialization of circuit nets.

The purpose in developing algebra is to provide for a concise well-defined framework for expressing and manipulating functions. In many applications, logic design in particular, a second and equally important consideration is that the operators of the algebra have simple and efficient circuit implementation[20].

Y

X \ F(X,Y)	0	1	2
0	0	1	2
1	3	4	5
2	6	7	8

Z Z Z

Y \ F(X,Y,Z)	0	1	2	0	1	2	0	1	2
0	0	1	2	9	10	11	18	19	20
1	3	4	5	12	13	14	21	22	23
2	6	7	8	15	16	17	24	25	26

X=0 X=1 X=2

Figure 2.1: Ternary map for 2 and 3 variable

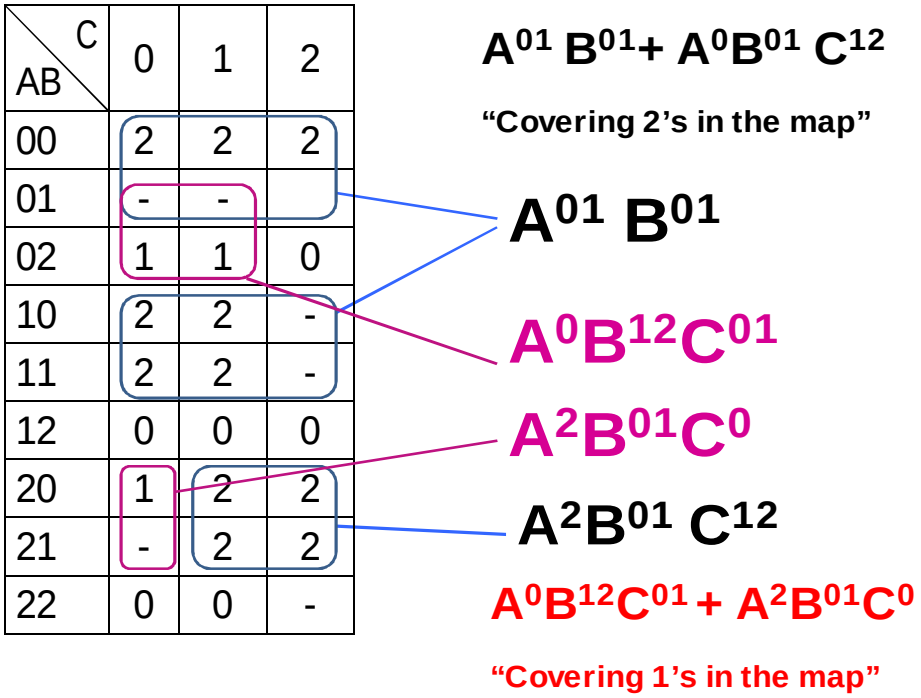


Figure 2.2: Example of ternary map for 3 variable

Binary Karnaugh maps are very effective for functions up to six variables. The key feature of binary K-maps is that only one variable changes when moving from a cell to an adjacent cell. The ternary map in figure 2.1and 2.2 has a similar property and depicts the representation of the 2 and 3 variables. In each square is entered the number of the minterm, which represents it

2.1.3 Ternary Logic Gates

Ternary logic family comprises of set of inverters, NOR gate and NAND gate. These circuits are used to design ternary memory elements and some basic ternary arithmetic circuits like half adder and full adders, and one-ternary multiplier. The circuits thus obtained are then used to synthesize a shift register, an N-bit adder, and an N-bit multiplier. Ternary NOT, NAND and NOR operations seem to be more important

as they are the building blocks of many other complex logical and arithmetic circuits. These fundamental logical functions can be defined in an m-valued k-variable system according to equations detailed below.

(i) Inverter

The Yoeli-Rosinfeld algebra [23] defines three basic ternary elements,

- Simple Ternary Inverter (STI)
- Positive Ternary Inverter (PTI)
- Negative Ternary Inverter (NTI)

Logically STI,PTI and NTI are formulated as,

$$STI = \overline{X^i} = 2 - X$$

$$PTI, NTI = \overline{X^i} = \begin{cases} i \rightarrow X \neq i \\ 2 - i \rightarrow X = i \end{cases} \quad \ldots\ldots \quad 2.1$$

Where, 'i' take the value of '2' for PTI and '0' for NTI inverter. Basic switching elements in the implementation of those inverters are transistors, MOSFETs& RTDs. Figure 2.3 shows the symbols of STI, PTI & NTI. Truth table for the same is given in Table 2.3.

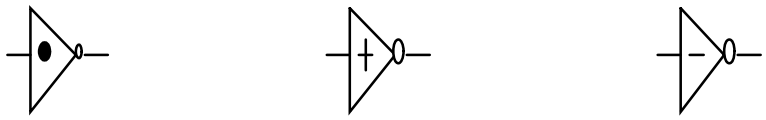


Figure 2.3: Symbols for Inverters (a) STI (b) PTI (c) NTI

Table 2.3: Truth table of Standard ternary gates

Input	**Output**		
X	**STI**	**PTI**	**NTI**
0	2	2	2
1	1	2	0
2	0	0	0

(ii) TOR and TNOR circuit

Ternary OR is a circuit that has X_1---X_n as input andY_o as output such that

$$TOR = X_1 + X_2 + ... + X_n = Max[X_1, X_2 ... X_n] \quad \text{..... 2.2}$$

Ternary NOR has an output that is a compliment of OR function i.e.

$$TNOR = \overline{X_1 + X_2 + ... + X_n} = \overline{Max[X_1, X_2 ... X_n]} \quad \text{.....2.3}$$

The sign + indicates logical ternary OR operation. Figure 2.4 shows Symbols for TOR/TNOR logic gates

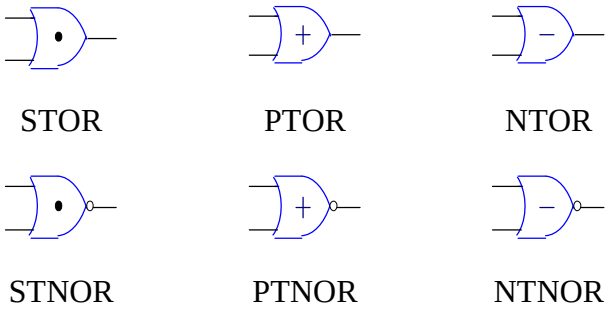


Figure 2.4: Symbols for TOR/TNOR logic gates

Inverter is a basic circuit that is used for implementing TOR/TNOR functions [23]. Depending upon the type of inverter used, the logic functions TOR/TNOR can be

- Simple ternary TOR/TNOR (STOR/STNOR)
- Positive Ternary OR/NOR (PTOR/PTNOR)
- Negative ternary OR/NOR (NTOR/NTNOR)

Table 2.4 shows the truth table of various ternary gates.

(iii) TAND and TNAND circuit

Ternary AND , Ternary NAND function is defined as

$$TAND = X_1 \cdot X_2 \cdot ..... \cdot X_n = Min\ [X_1, X_2, ... X_n] \quad \text{.....2.4}$$

$$TNAND = \overline{X_1 \cdot X_2 \cdot ..... \cdot X_n} = \overline{Min\ [X_1, X_2, ... X_n]} \quad \text{.....2.5}$$

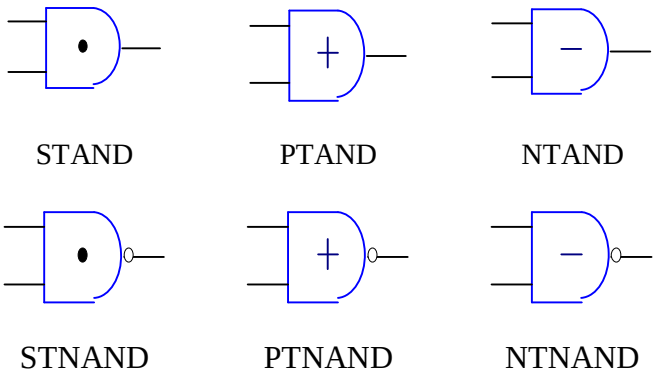


Figure 2.5: Symbols for TAND/ TNAND logic gates

Table 2.4: Truth table of the Ternary gates

A	B	TNAND	TAND	TNOR	TOR	TXOR	TXNOR
0	0	2	0	2	0	0	2
0	1	2	0	1	1	1	1
0	2	2	0	0	2	2	0
1	0	2	0	1	1	1	1
1	1	1	1	1	1	1	1
1	2	1	1	0	2	1	1
2	0	2	0	0	2	2	0
2	1	1	1	0	2	1	1
2	2	0	2	0	2	0	2

Figure 2.5 shows Symbols for TAND/TNAND logic gates.Depending on the type of inverter used, the logic functions TAND/TNAND can be

- Simple ternary TAND/TNAND (STAND/STNAND)
- Positive Ternary AND/NAND (PTAND/PTNAND)
- Negative ternary AND/NAND (NTAND/NTNAND)

2.1.4 Switching Devices For The Realization Of Ternary Logic

Complementary Metal Oxide Semiconductor (CMOS) has been the predominant technology of the past two decades to implement ternary and other MVL systems. Several types of CMOS-based MVL circuits have already been proposed in the literature as the emerging of MOSFET technology. However, they are unsuitable for the current and the upcoming technologies [6]. This encouraged the introduction of some beyond-CMOS nanodevices such as Carbon NanoTube Field Effect Transistor (CNTFET)[6,1], Quantum-dot Cellular Automata (QCA), Single Electron Technology (SET)[6] and Quantum Dot Gate FET (QDGFET) [15] for MVL systems. These nanodevices benefit from low-power consumption, ballistic transport attributes under low supply voltages and very small sizes that make them very suitable for ultra-low-power, ultra-high-performance and ultra-high-density chip design [6]. They are considered as a promising choice for future computing technology in many areas including MVL. The present research interests are therefore focused on investigating the utility of such devices for designing ternary systems.

2.2 Multi Input Floating Gate MOSFET (MIFG)

Advancement in VLSI technology has allowed for doubling component density on a silicon chip after every three years. Though MOS transistors have been scaled down, increased interconnections have limited circuit density on a chip. It has become essential to explore other methods of adding more functionality to a MOS transistor. Multiple Input Floating Gate (MIFG) MOS transistor is one such switching device which has made it possible to implement ternary circuits using fewer transistors and reduced interconnections. A novel

approach based on utilization of MIFG MOS transistor for the realization of the ternary circuits is a major contribution of this research. The theoretical foundations of MIFG are detailed in this section.

2.2.1 MIFG As A Switching Device For Realization Of Ternary Circuits

MIFG is a functional MOS transistor that works more intelligently than a mere switching device. The functional transistor calculates weighted sum of all input signals at the gate level, and controls the "ON" and "OFF" state of the transistor based on the result of such a weighted sum operation. The proposed research aims to explore the usefulness of MIFGMOS transistor for the design and simulation of ternary logic circuits.

The floating gate voltage is proportional to the stored charge and the charge is proportional to the input voltages capacitively coupled. Upon modifying the charge, the floating gate voltage will change. So, the current through the transistor also will change according to the input voltages. This makes it possible to achieve the desired third state as defined in case of a ternary logic. The device thus outperforms when explored from the ternary perspective. It is similar to MOSFET in terms of inherent electronic characteristics. On account of this similarity, previously designed structures based on CMOS platforms can still be utilized in MIFGMOS transistor based design. MIFG, as explored in this research proves to be an efficient switching device for the realization of the ternary circuits. Figure 2.6 depicts the symbol of MIFG.

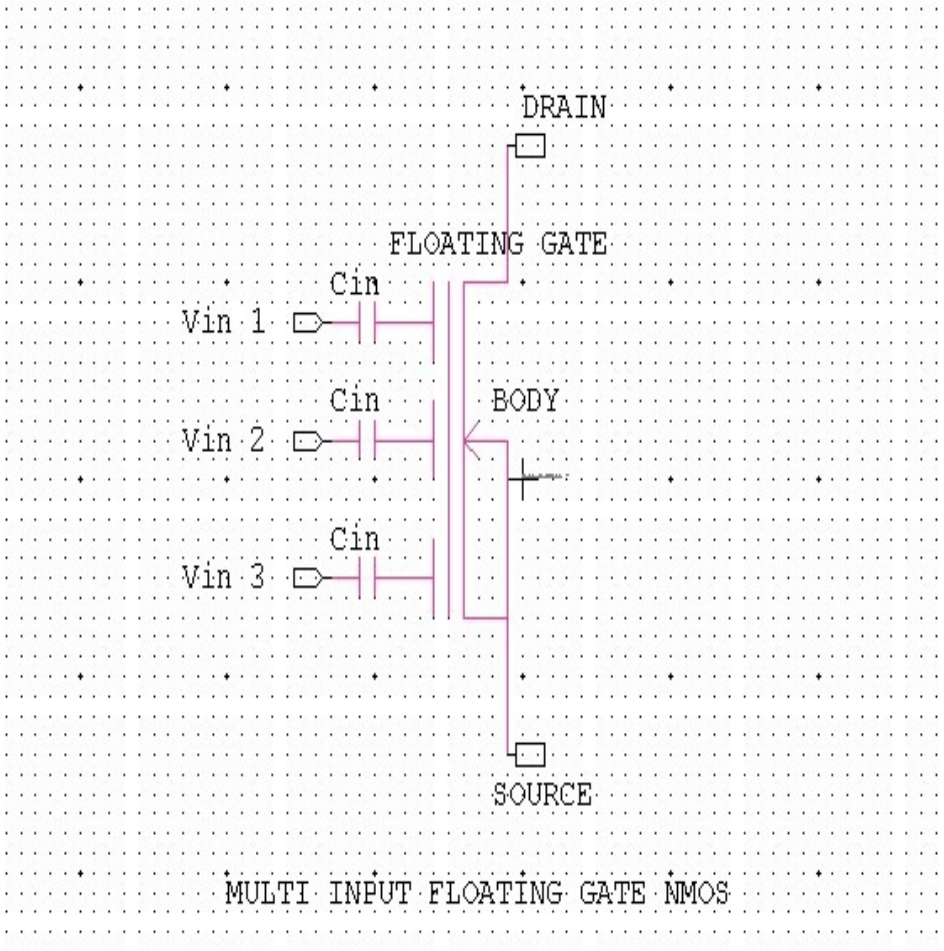


Figure 2.6: MIFG MOSFET Symbol

2.2.2 Structure Of MIFG

The structure of MIFG MOSFET, as shown in Figure 2.7 comprises of the floating gate and number of input gates built on poly2, which is coupled to poly1 gate by capacitors between poly1 and poly2. This structure makes it possible for multi- input floating gate devices to be implemented in double polysilicon CMOS process. The floating gate in the MOSFET extends over the channel and the field oxide. A number of control gates, which are inputs to the transistor, are formed over the floating gate using a second polysilicon layer (poly 2) [24].

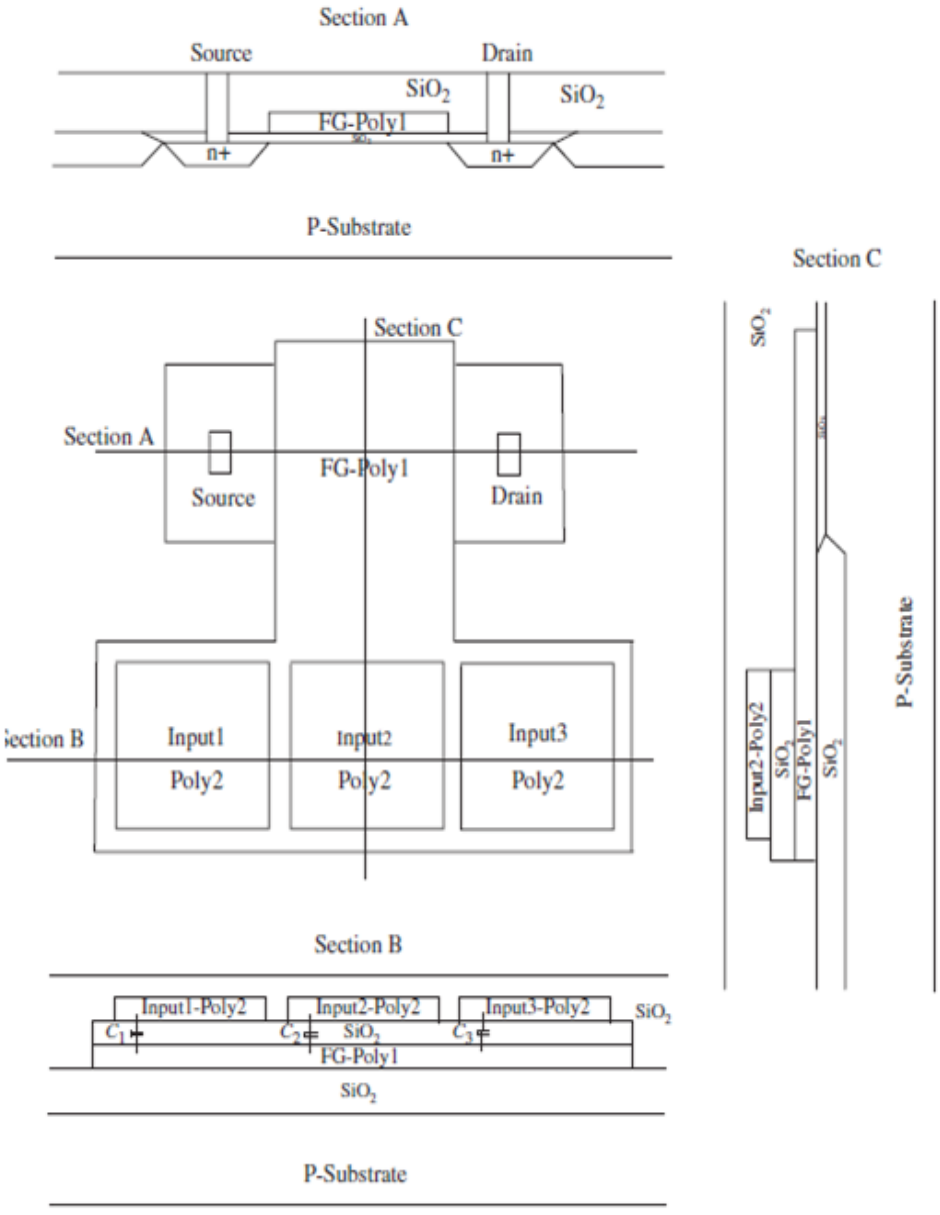
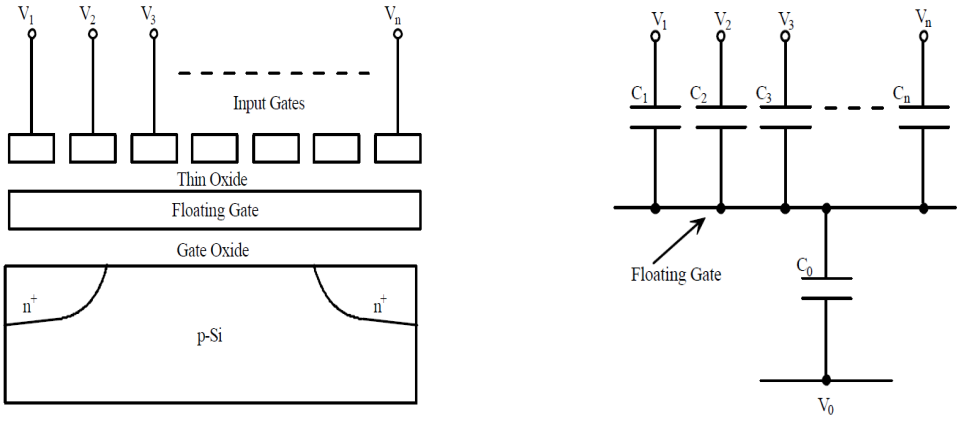


Figure 2.7: Possible Layout Of a 3-input n-channel FGMOS transistor(middle) and its cross-sectional views (A, B and C)[25]

The device is composed of a floating gate and multiples of input gates that are capacitively interacting with the floating gate. As the gate-level sum operation is performed in a voltage mode utilizing the capacitive coupling effect, essentially no power dissipation occurs in the calculation, making the device ideal for ULSI implementation.



(a) (b)

Figure 2.8: Simplified structure of MIFGMOS transistor

Figure 2.8 depicts a simplified structure of MIFGMOS transistor [26]. They have the same basic properties as equivalent to ordinary MOS transistors but widened by certain additional features. The most significant of them, there is the ability of summing gate controlling input signals as well as the possibility of reduction of threshold value voltage [26]. Let V_{th} be the threshold voltage of the transistor. The transistor turns on at the condition where the potential at the floating gate exceeds the threshold voltage, i.e. $\emptyset_F > V_{th}$, and is described by the eq. 2.6 and 2.7 [26]

$$\emptyset_F(t) = \emptyset_F(0) + \frac{\sum_{i=1}^{n}(C_i V_i(t) - C_i V_i(0))}{\sum_{i=0}^{n} C_i} \quad \ldots\ldots\ldots \quad 2.6$$

Where,

n is the number of inputs

$\emptyset_F(t)$ is the potential at the floating gate

V_{th} is the threshold voltage

$$\frac{V_1 C_1 + V_2 C_2 \ldots\ldots\ldots V_n C_n}{C_1 + C_2 \ldots\ldots\ldots C_n + C_0} > V_{th} \quad \ldots\ldots\ldots 2.7$$

These transistors can operate as normal MOS as saturated or non-saturated within the region of strong inversion or typically within the region of weak inversion called sub-threshold region. That second operating region is utilized in electronic circuits with very low supply voltage [27].

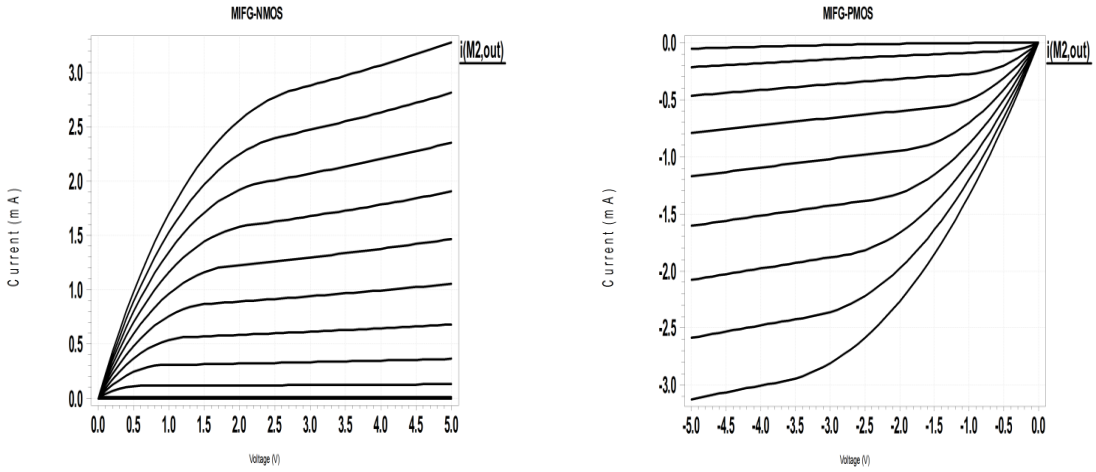
Figure 2.8(a) shows capacitive coupling between the multiple-input gates and floating gate and the channel. Figure 2.8(b) C_1, C_2, C_3 and C_n are the coupling capacitors between the floating gate and the inputs. The corresponding terminal voltages are V_1, V2, V3,…,Vn, respectively. C_0 is the capacitor between the floating gate and substrate. VSS is the substrate voltage. Q_1, Q_2, Q_3, …,Qn are the charges stored in corresponding capacitors C_1, C_2, C_3, …, Cn.

The multi-input floating gate MOSFET operation depends on the weighted sum of voltages at input nodes, which are capacitively coupled to the gate.

2.2.3 IV Characteristics of MIFG

Figure 2.9 shows the output IV characteristics of n channel and p channel MIFGMOS transistor operated under identical voltage levels i.e. 3V, which confirm the design considerations of the proposed approach. Eq. 2.8, 2.9 and 2.10 represent the modeling equations of the MIFGMOS transistor [26].

As clear from the characteristics and the modelling equation, the three operating region of MIFGMOS transistor are cut off, strong inversion ohmic and strong inversion saturation. In cut-off region, gate to source voltage, V_{gs} is less than the threshold voltage V_{th} and no current flows through the device making it act like a open switch. Whereas in strong inversion ohmic region, V_{gs} is greater the $V_{th}$and the device behaves like a resistor. In strong inversion saturation region, the device is fully ON and behaves as closed switch.



(a) (b)

Figure 2.9: IV characteristics of (a) nMIFGMOS transistor (b) pMIFGMOS transistor

Cut off region

$I_D = 0$

$V_{GS} < V_T$ 2.8

Strong Inversion Ohmic region

$$I_D = \frac{\beta}{2}\left\{\left[\left(\sum_{i=1}^{N}\frac{C_i}{C_T}V_{iS} - \left(V_T - \frac{C_{GB}}{C_T}V_{BS} - \frac{Q_{FG}}{C_T}\right)\right)\right] - \left(\frac{1}{2} - \frac{C_{GD}}{C_T}\right)V_{DS}\right\}$$

For

$$0 < V_{DS} \le \left(\sum_{i=1}^{N}\frac{C_i}{C_T}V_{iS} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS} + \frac{Q_{FG}}{C_T} - V_T\right)$$

$V_{GS} > V_T$ ...2.9

Strong Inversion Saturation region

$$I_D = \frac{\beta}{2}\left(\sum_{i=1}^{N}\frac{C_i}{C_T}V_{iS} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS} + \frac{Q_{FG}}{C_T} - V_T\right)^2$$

For ...2.10

$$0 < \left(\sum_{i=1}^{N}\frac{C_i}{C_T}V_{iS} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS} + \frac{Q_{FG}}{C_T} - V_T\right) \le V_{DS}$$

$V_{GS} > V_T$

Several effects can be observed from these equations:

- The floating-gate transistor can go into depletion-mode

operation and can conduct current even when |*VGS*| <|*VT*|. This is because the channel can be turned on by the drain voltage through the *f VDs*.

- Region 2 for the conventional MOS transistor is the saturation region where $I_{DS}$is essentially independent of the drainvoltage. This is no longer true for the floating-gate transistorin which the drain current will continue to rise as the drainvoltage increases and saturation will not occur.

The floating gate voltage is proportional to the stored charge and this is further proportional to the input voltages capacitively coupled. Upon modifying the charge, the floating gate voltage will change. So, the current through the transistor also will change according to the input voltages thus making it possible to achieve the desired states in the ternary logic.

2.2.4 Concept of Variable Switching Voltage in MIFG

The conductivity of the floating-gate MOS transistor differs from that of a conventional MOS transistor having the same applied terminal voltages due to a capacitive coupling between the drain region and the floating gate. When a voltage is applied to the drain region, capacitive coupling between the drain and the floating gate induces a high electrical potential on the floating gate. This induced field on the floating gate then modifies the conductivity of the underlying channel region.The uniqueness of multi-input floating gate MOSFET lies in the fact that the switching voltage can be varied by selection of those capacitor values through which the inputs are coupled to the gate. In conventional MOSFET, varying the W/L ratios of the MOSFET varies the threshold voltage. In multi- input floating

gate MOSFET, varying the coupling capacitances to the gate can vary the switching point in DC transfer characteristics.

By providing various fixed input voltages at different gates, the floating gate voltage, Φ_F can be varied thereby adjusting the charge on the floating gate. The input voltage at the floating gate is the weighted sum of all the individual input voltages, with the capacitances acting as the weights. So, by fixing the input voltage at a gate to either V_{DD} or GND, the average input voltage can be varied effectively varying the threshold voltage level of the PMOS and NMOS MIFG transistor pair. Hence, the output switches its state at different input voltages just as it would if the W_p/W_n ratio were to be varied.

This ability to alter the charge during operation on a floating gate transistor allows its effective utilization in realization of the multi valued logic circuits.

2.3 Review of Digital Ternary Logic Systems

With the development of MVL by ***Post*** and ***Lukasiewicz*** in 1920, several attempts have been made to use this concept in computer science [16]. Since ***R.E. Miller(1965)***proposed in his book on “switching theory, John wiley , 1965” that base three system is most efficient number system, the concept of the ternary based computations and the required algebra was developed. ***Yoeli et al.*** [28] developed the algebra for logical design of ternary switching circuits and attracted the interests of many researchers [29]. An excellent review of the first developments of MVL and its application to electronics, including a few circuit implementations was presented by ***Epstein et al.(1974)*** [7] considering the area of MVL was an emerging thrust area with special focus on ternary logic. Ternary functions were studied in detail from the standpoint of their functional

completeness or representations.

Mukaidono et al. (1981) introduced some special subsets of ternary functions called regular, normal and uniform. When applying the ternary functions to various fields of engineering, it is seldom that all the functions are used. So only some subsets of ternary logic were identified in their research with special properties and meaning. These ternary functions are popularly used in various field of engineering like switching theory, programming languages, algorithm theory and many other fields [30]. Ternary logic was thus continued to be explored to replace binary logic and other applications.

Bala et al. (1984) proposed a MOS ternary-logic family, which is comprised of a set of inverters, NOR gates, and NAND gates. These gates are used to design basic ternary arithmetic and memory circuits. The circuits thus obtained are then used to synthesize complex ternary arithmetic circuits and shift registers. The ternary circuits developed are shown to have some significant advantages relative to other known ternary circuits like low power dissipation, and reduced propagation delay and component count. For a given dynamic range, the complexity of the new ternary circuits is shown to be comparable to that of corresponding binary circuits. Nevertheless, the associated reduction in the word-length in the case of the ternary circuits tends to alleviate to a large extent the pin limitation problem associated with VLSI implementation. The cyclic convolution, an application is implemented in which a significant advantage can be gained through the use of ternary digital hardware [9].

With the recent technological advancements, commercial realization of ternary circuits is watched with keen interest. Literature

reports various simulation tools like SPICE and VHDL simulator to design various building blocks and fundamental elements of a ternary processor.

Mouetal. (1986) proposed a new scheme in which ternary clocking signals are used to replace the binary clocking signals in VLSI scan testing designs. The clocking scheme exploits the ternary logic to eliminate the mode selecting line and reduce the interconnection problem and the chip area and has the same advantage of high testability as the binary scan method. [31]

Seger et al.(1988) presented one such application of ternary logic in developing a model for detection of timing problems in digital networks. The ternary logic based model is closely related to the binary almost-equal-delay-model and is considerably more efficient. It could also be easily incorporated in the simulators [32]. The novel ternary algorithm is capable of detecting critical races under the assumption that all delays are approximately but not exactly equal. A major disadvantage with the ternary algorithm is that it is not guaranteed to halt, leading to an argument that a practical circuit that does not stabilize in say, ten races is not very well designed.

Wang et al. (1988)developed a new dynamic ternary logic and its circuit structures to achieve the goal of low power dissipation and high operation. The devised approach implements YoeliRosenfield algebra however, needs four phase clocking scheme. The dynamic CMOS ternary logic has advantages of low power, small area and high speed. Moreover, it can be implemented by the CMOS process used by the binary circuits[29]. In another research by ***Morisue et al.***

(1989)Josephson junction and its tri-stable-state has been utilized to construct several circuits in ternary form [33, 34].

Rizvi et al. (1991)on the other hand designed a spatial filtering Location Addressable Memory [LAM] in ternary logic that is capable of handling multi-input multi-output in an efficient way. The LAM device can be used in the truth table lookup implementation processor in ternary logic. The devised approach is validated by implementing ternary combinational circuits like ternary half adder and ternary Subtractor [35].

Rozan et al. (1996) utilized*, VHDL simulator,* a hardware description language, as a potential tool for the simulation of MVL logic circuits and systems. The work demonstrates how VHDL can be used as a potential tool for the simulation of multi-valued digital circuits and systems. Although not all features of a given VHDL simulator can be applied to MVL signals, some can easily be adapted to provide enough information to verify functionality and/or timing specifications. The VHDL modeling and simulation of two simple ternary circuits are described and commented [10].

Jones et al. (1996)focused his research on ternary algebra and modeling to discuss the simultaneous existence and relationships, between binary and ternary. Their research defined the various interpretations and rules that can be applied to the simultaneous existence. Finally the formulated rules were utilized the further implicit dynamics of ternary relationships when multiple binary relationships are imposed [36].

Masahiro et al. (1997) presented a novel ternary fuzzy processor using the logic oriented neural networks. The simulation results are illustrated to show how a ternary fuzzy inference engine can be realized by taking into consideration of advantages of neural networks. The principle to construct a ternary processor using the neural networks is described in detail and the simulation results for a novel Max circuit which is the essential circuit of the fuzzy inference engine are given. The features of the proposed processor are capability of high speed operation, and very simple construction with less number of elements to perform a function of fuzzy processor [4].

Serran et al. (1997)presented a proposal for the implementation of ternary digital circuits. Their study described a new multivalued algebra that uses the Post's cyclic negation, the AND conjunction and new operators which allow the development of simple algorithms for the synthesis and simplification of the logical function.An electronic implementation of a ternary logic is also presented in their investigation [37].

Srivastava et al. (2000) on the other hand implemented the ternary functions mainly by adjusting the W/L ratios of the transistors in a CMOS inverter and by using a transmission gate at the output. Back-gate bias provides an additional parameter in the design of CMOS ternary logic circuit for the low voltage operation to generate the desired DC voltage transfer characteristics and transition region adjustment. Key building blocks – a STI, PTI and NTI are designed using the proposed method [38].

Nascimento et al. (2001) attempted to design a perfect automated tool for analysis and design of MVL digital circuits. They presented software called *ELOmv*, is capable of calculating the truth table for expressions in ternary or quaternary level with even three variables of entry. This software is a tool that can be used in a future work in which synthesis and simplification of logical functions will be performed [39].

Yamamoto et al. (2003) defined an extension of the ternary majority function using cyclic operation to I/O values of the function. The extended ternary majority functions are functionally complete on a ternary logic system and enable the representation of any ternary logic. Genetic Algorithm (GA) is used as a tool and an advanced method applicable to many variable case is proposed together with some experiments [40].

Maddess et al. (2004) explored the utility of ternary logic for texture representation. A systematic method for producing texture pattern is recognized for creating a large number of classes of binary (256) and ternary (7.62×10^{12}) textures. Their study presents guidelines and analytical methods for selecting sets of textures with particular image qualities and non-linear relationships between pixels. Given the large number of patterns, there are undoubtedly many applications other than image processing and pattern recognition that demand the wide patterns for representing the two or three brightness levels or colors[41].

Raychowdhury et al. (2004) 2004 presented a novel method of multiple-valued logic design using CNTFETs. The geometry dependant

threshold voltage of these transistors has been used to design a ternary logic family HSPICE has been used in all simulations and transient as well as dc characteristics have been studied [18].

Gundersen et al. (2005) explored the switching devices for the realization of ternary circuits. A novel voltage non-inverting CMOS Semi-Floating- Gate (SFG) ternary switching element is presented. This element shows good noise margin and is easy to fine tune, and it is well suitable to use in refreshing ternary signals in memory applications. [42].

Dhande et al. (2005, 2007) exploited the existing VHDL as a potential EDA tool for the simulation of MVL circuits and system by considering signal 'Z' as one of the state of MVL system along with signals '0' and '1'(0 being ground potential, Z intermediate state and 1 as +5v state). The VHDL modelling and simulation of T-Gates and 1-bit multiplier circuit is described and commented. The architecture, design and implementation of 2 bit ternary ALU (T-ALU) slice are also described. The proposed ALU is designed for two-bit operation & can be used for n bit operations by cascading n/2 ALU slices. The designed technique used here requires only two stages i.e. decoder & T -gates, as against three stages i.e. decoder, binary gates & encoder require in conventional ternary logic implementation. is suitable for LSI / VLSI implementation [11,12].

Haider et al. (2008)introduced a new set of ternary neural networks to realize a novel Ternary Arithmetic and Logical Unit (TALU) using *MATLAB Simulink* as a simulation tool to demonstrate the feasibility, functionality and the correctness of the neural network design [43].

Romero et al. (2009) proposed algebra based on a universal set of gates which carry out operators to allow synthesis and simplification of MV logic digital circuits. Their research address the generated algebra, the algebraic form of the function to be synthesized based on the canonical form of sum of product terms, the duality and circuit simplification procedures. Combinational and sequential circuits are synthesized to demonstrate the correctness of the algebra. The proposed algebra allows designing any MV logic digital circuits by extending it to the MV logic digital circuit designing [23].

Sadik et al. (2009) presents novel 1-trit ternary arithmetic structures. The input, internal processing and the output are entirely in the ternary domain. The operation of the proposed adder is assessed in terms of the accuracy which is expressed as the equivalent number of bits in corresponding multibit system. Furthermore, based on the analysis of its operation, a technique has been proposed to design better performance versions. This led to the design of1-trit integrators. Both the circuits present promising performances. It is necessary to extend the approach to realize multiplication, division and exponential functions [44].

Satishkumar et al. (2010) have presented a novel method for defining, analyzing and implementing the basic combinational circuitry with minimum number of ternary multiplexers. Multiplexer is used as basic building gate to realize all the sequential and combinational circuitry which provides complete, concise, implementation-free description of the ternary functions involved. The method is useful in analyzing the complex ternary functions and reduction of gate count [45].

Sheng et al. (2011) presents novel design of ternary logic gates using Carbon Nano Tube (CNT) FETs (CNTFETs). A resistive-load CNTFET-based ternary logic design has been proposed to implement ternary logic based on CNTFET and compared with the existing resistive-load CNTFET logic gate designs. Especially, the proposed ternary logic gate design technique combined with the conventional binary logic gate design technique provides an excellent speed and power consumption characteristics in data path circuit such as full adder and multiplier. Extensive simulation results using SPICE are reported to show that the proposed ternary logic gates consume significantly lower power and delay than the previous resistive-load CNTFET gates implementations. In realistic circuit application, the utilization of the proposed ternary gates combined with binary gates results in over 90% reductions in terms of the power delay product [1].

Supriya et al. (2013) discuss logic circuit designs using the circuit model of three-state Quantum Dot Gate Field Effect Transistors (QDGFETs). QDGFETs produce one intermediate state between the two normal stable ON and OFF states due to a change in the threshold voltage over this range. A simplified circuit model that accounts for this intermediate state is developed. The designs of various two-input three-state QDGFET gates, i.e. ternary gates, including NAND- and NOR-like operations and their application in different combinational circuits like decoder, multiplier, adder are presented. Increased number of states in three-state QDGFETs will increase the number of bit-handling capability of this device and will help us to handle more number of bits at a time with less circuit elements [13]. Table 2.5 summarizes the circuit elements used in the CNTFET and QDGFET

based approaches.

Moaiyeri (2013) presented low-power MVL circuits for nanoelectronics. CNTFET-based MVL circuits are designed based on the unique characteristics of the CNTFET device such as the capability of setting the desired threshold voltages by adopting correct diameters for the nanotubes as well as the same carrier mobility for the P- and N-type devices. The method proposed in this study is a universal technique for designing MVL logic circuits with any arbitrary number of logic levels, without static power dissipation. The results of the simulations, conducted using Synopsys HSPICE with 32 nm-CNTFET technology, demonstrate improvements in terms of power consumption, energy efficiency, robustness and specifically static power dissipation with respect to the other state-of-the-art ternary circuits [6].

Yan-Feng Lang (2014) proposed a Ternary Clock Generator (TCG) to settle its shortage. The TCG is implemented at the switch level with a simple structure of 24 MOS transistors and simulated at the layout level using the HSPICE software with TSMC 0.18 μm CMOS technology, showing that it works properly. The analyses show that the proposed TCG not only can output a ternary clock of high quality, meeting the clock's design requirements, but also can be fabricated with standard CMOS technology [46].

Table 2.5: Number of circuit elements used in CNTFET and QDGFET based approaches

No of Components	**STI**		**NAND / NOR**		**TERNARY DECODER**	
	CNTFET	QDGFET	CNTFET	QDGFET	CNTFET	QDGFET
	6	2	10	4	16	10

The literature survey thus highlights the significance and the developments in MVL thus making it thrust area of research. With the recent technological advancements commercial realization of MVL circuits is watched with keen interest and has gained wide popularity. The prime objective of this research work is to develop, simulate and test the ternary logic circuits and propose ternary logic processor architecture.

2.4 A Brief Review of MIFGMOS Transistor

This research presents a novel MIFG based approach for the realization of the ternary circuits. This section presents the developments in the MIFGMOS transistor.

With the increasing demand for smaller and faster products, there is an ongoing trend in fabrication process towards smaller transistors. In the quest to achieve low-voltage and low-power, various techniques have evolved in due course of time and MIFGMOS transistor technique is one amongst them [47]. Due to the special characteristics of the MIFGMOS transistor, its application in both analog and digital circuits has been very wide since the first report in 1967. The first well-known application of the MIFGMOS was to store data in EEPROMs, EPROMs and FLASH memories. During the last ten years, a number of different applications have revealed possibilities that this device could have in many other different fields [26]. *Abhinav et al*. designed a new

current mirror with MIFGMOS which exhibit high output impedance, higher current range, very low power dissipation and higher matching accuracy [47, 48]

A number of interesting applications have also been exploited in digital circuits. It is demonstrated that a MOSFET having an externally adjustable threshold voltage is quite essential for implementing a [20]. Other advantages listed below also make MIFGMOS transistor a competent candidate for the realization of ternary logic [26, 47].

- From the implementation point of view, MVL designs must be compatible with the existing binary technologies. MIFG MOS transistors can be very well implemented in lieu of conventional MOSFET.
- Incredible features of flexibility, controllability and tunability of MIFGMOS transistor yields better results with respect to power, supply voltage and output swing.
- A control voltage present at the MIFGMOS transistor and facility of additional weighted inputs provides wide range of tunability to the circuit.
- Implementation of MIFGMOS transistor allows threshold voltage (V_{th}) controllability without reducing the feature size. Also, it consumes less power than the minimum required power for a circuit designed with conventional MOSFET.
- Simplifies the topology of the digital systems

For digital circuits, MIFGMOS transistor has thus been considered to be a potentially better technique than standard static CMOS Circuits [25]. Exploring the MIFGMOS for the design of efficient ternary circuits is the major focus of this research.

2.5 Challenges and Limitations of Existing Systems

Following are the major challenges, limitations and unidentified issues in thedevelopment of ternary logic.

- **Only a limited soft computation and Artificial Intelligence approaches are explored**:

The literature reports wide assortment of various methods used for the development of the ternary circuits. The soft computation approaches are not fully explored to validate its efficiency and usability for the realization of ternary circuits. Literature reports use of neural network and fuzzy to a limited extent. The reported neural networks do not consider or address the major issue of catastrophic forgetting to design intelligent systems. Efficient use of Fuzzy Inference Systems (FIS), Adaptive Neuro-Fuzzy Inference System (ANFIS) to take advantage of fuzziness in terms of the levels, genetic algorithm, Artificial Intelligence approaches and other supervised and unsupervised algorithms are likely to deliver improved results and need to be further explored.

- **Limited functionality and performance analysis of the simulated ternary circuits:**

Most of the studies present encouraging simulation results but are limited only to a few typical operations. It is of utmost importance to further extend them and include a variety of other scalar and vector arithmetic and logical circuits, which is imperative for a ternary processor. Moreover, the studies presented in [3,10,39] do not consider the timing issues. The prorogation delay plays a crucial role especially in ternary arithmetic and logical operations. It is important to therefore consider it and examine the simulation results accordingly. It is also necessary to include other important issues like

instruction set, clock and control signals in the implementation and the simulation of the circuits from the context of a ternary processor.

- **CMOS based approach are popularly used without addressing its major disadvantages:**

CMOS based approaches are popularly used for the realization of ternary circuits. However the CMOS based approach is reported to have many disadvantages like

- high static power
- requirement of large off-chip resistors
- need of multiple supply voltages
- use of depletion-mode MOSFETs

These drawbacks outweigh its advantages and make them unsuitable for the upcoming technologies [12]. As reported by *Plummer et al.* [14] the upcoming era will be dominated by beyond CMOS devices.The encouraging results and the limitations in the state of art methods continue to draw attention of the research community and demand further researches to investigate the simulation based approaches and also explore the suitability of other beyond-CMOS devices for the implementation of ternary logic.

- **Use of CNTFET based approach**

Some of the popular beyond CMOS devices like, the CNTFET are successfully used for the ternary circuits but suffer from

- large circuit elements
- misaligned and mis-positioned CNTs
- high resistance CNT metal contact
- chemical doping
- fabrication issues
- Integration issues of N- and P- type CNTFET on the same

substrate.

CNTFET based designs demand further research in order to obtain complementary VLSI CNTFET based circuits. Moreover, even the reported CNTFET designs that combine use of ternary and binary gates for design of ternary combinational need additional investigation [6]. The reported studies cite the use of binary CNTFET gates and claim to achieve reduction in the circuit element count. However the research does not detail design, implementation and the simulation of Binary CNTFET based gates [6]. Thus additional research is required to explore the CNTFET for the realization binary gates.

- **Functionality issue in the design of QDGFET based Ternary full adder:**

The QDGFET based circuits [13] are designed **using the depletion MOSFETs**, which are obsolete these days and will need additional chip area in the fabrication process. Moreover The QDGFET designs utilize a supply of 500mV, which helps them to achieve less PDP but the noise margin is compromised significantly.

Another major concern in the QDGFET based Ternary Full Adder (TFA), presented in their research is its functionality issue.The waveforms for various input-output combinations are depicted in [13] which confirm the functionality of the reported approach. A careful debugging of the circuit proposed in paper reveals a functionality issue in the design of full adder when A= B = C_{in} ='2'. The reported design of TFA does not consider the realization of the term $A^2B^2C^2$ and thus suffers from a functionality issue. This limitation will be detailed further in section 3.6.2. The reported design of TFA needs a careful examination to verify its operation for all the combinations of the input.

- **Meager attention to design of Ternary Level Shifter [TLS]**:

Irrespective of the balanced or unbalanced systems, a TLS (also called as T-buffer) is a vital component in the realization of ternary digital circuit. It shifts the higher voltage (logic state '2') to intermediate voltage level (logic state '1'), thusgiving the output of 2.5 V (forunbalancedternarysystems) or 0V (forbalancedternary). However, the design of TLS has recievedless attention by the researchers. The reported TLS use an additional power supply in their designs. An additional power supply and passive components function as voltage divider to obtain the required voltage of $V_{DD}/2$. This obviously leads to the power consumption issues related to the voltage divider circuit. Moreover there are limitations of the voltage divider to act as precise reference. To overcome these limitations it is imperative to further investigate the TLS based designs.

- **Meager attention to design of ternary sequential circuits**

The reported studies and investigations in development of ternary logic focused on combinational circuits and they need to be further extended for sequential circuits. Relatively skimpy studies are presented detailing the flip-flap-flops, shift registers, memories and counters. The sequential circuits are important components of a processor and their design, implementation and simulation is therefore necessary from the perspective of a ternary processor. Moreover investigations to identify race around and lock-out conditions, hazards detection and diagnosis will be useful when designing a ternary processor.

- **Simulation tools and VHDL based modeling are not fully exploited to design flexible ternary circuits**:

The programming languages like VHDL needs to be efficiently utilized and the advantage of the language should be exploited for better performance analysis of the ternary circuits. Simulation tools like VHDL only demonstrate the functionality of the devised circuits without considering the challenges from the realization prospective and may lack sufficient detailed information of the device. It is necessary to consider a variety of operations and timing delays during the simulation of ternary circuits. Additionally,In most of the studies, there still remains out-sized scope to evaluate the reductions techniques in digital designing, especially for the ternary circuits. This may further give additional circuit reduction, thereby reducing the delays and the complexity in VLSI designing.

The literature thus reports wide contributions in the VHDL simulation based approaches and device level realizations of various ternary circuits. Despite the potential advantages of ternary logic over the binary, realization of an efficient, realistic and a practical ternary processor is still a thrust area of research. This research aims to address some of these challenges and unidentified issues in the design of ternary processor.This research addresses some of these challenges and unidentified issues.

Chapter 3

SWITCHING DEVICES FOR THE REALIZATION OF VARIOUS TERNARY CIRCUITS

Complementary Metal Oxide Semiconductor (CMOS) has been the predominant technology of the past two decades to implement ternary and other MVL systems. Several types of CMOS-based MVL circuits have already been reported in the literature as the emerging of MOSFET technology. In addition to the mainstream CMOS device, many newly emerging devices show potential for use in implementation and realization of the logic circuits that inherently support ternary logic. The present research interest is inclined to explore several beyond CMOS devices are considered as a promising choice for future computing technology for ternary logic. This chapter details the highlights and the major contribution of this research as listed below:

- CMOS based ternary gates are designed and simulated to initially revalidate the functionality and examine the limitations.
- MIFGMOS transistor is explored to design and simulate basic binary gates (AND and OR).
- A novel hybrid approach based on combination of MIFGMOS transistor and conventional MOSFET is further devised to overcome the limitations of the CMOS based approach and realize the basic ternary gates (TAND and TOR).

- A modified ternary decoder is designed that achieves reduction in circuit element count as compared to the state of the art approaches.
- A novel Ternary Logic Shifter (TLS), which has received meager attention by researchers, is designed and extensively simulated to verify its operation.
- Functionality issue in the reported design of Ternary Full Adder (TFA) is identified and a solution to the identified problem is implemented.
- Design and simulation of MIFGMOS transistor based TALU with ternary combinational circuits is realized using the modified decoder, novel TLS and only ternary gates.
- The performance of designed TALU is further improved using the combination of ternary and binary gates.
- Finally the ternary sequential circuits are also designed and simulated from a ternary processor perspective.

3.1 MOSFET Based Approach

CMOS has been a dominant technology for the implementation of the binary logic circuits. Few CMOS-based ternary circuits have already been reported earlier by the researchers. However, it is necessary to verify the functionality and examine the limitations of the CMOS based approach for realization of the ternary logic circuits so as to explore other switching devices for better suitability.

3.1.1 Research Methodology to Design MOSFET based Ternary Gates

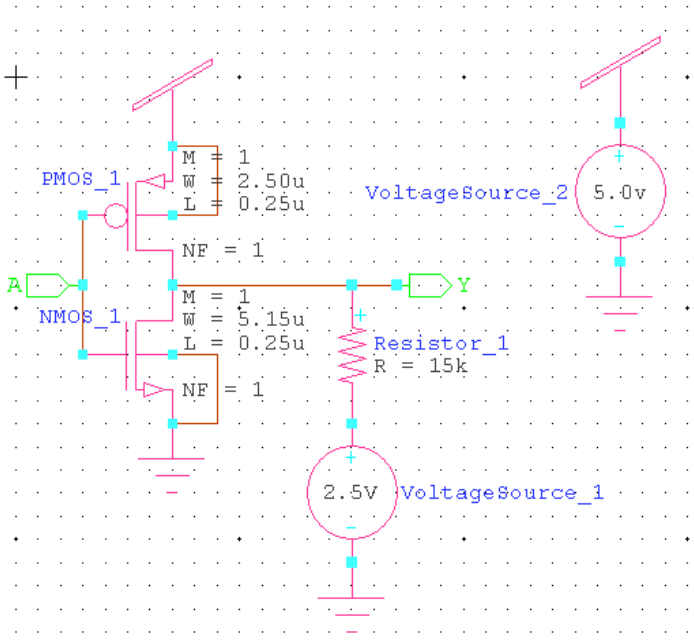
The research methodology to design the CMOS based ternary logic circuits encompass a conceptual transformation of the original

binary logic diagram of the circuit into the corresponding ternary ones using the injected voltage method [49]. Unbalanced or Ordinary logic with three voltage levels (0 V, 2.5 V, 5V) are used to represent three ternary logic levels (0, 1, 2).

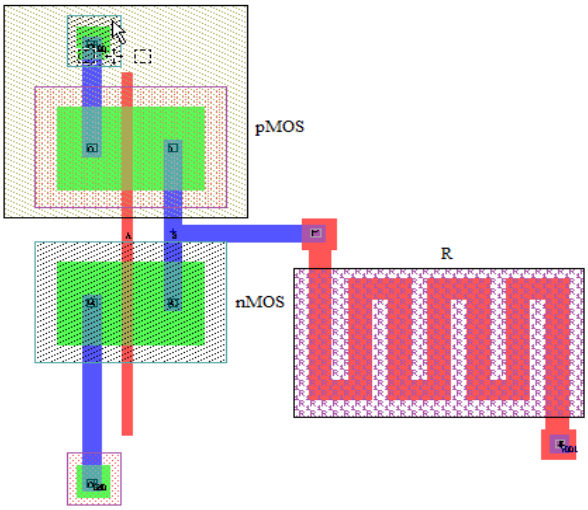
Figure 3.1(a) depicts a simple ternary inverter (STI) which is composed of nMOS, pMOS and a resistor 'R'. voltage source$_1$, $V_{DD}$is 5V and auxiliary power supply, voltage source$_2$ is 2.5 V. The absolute values of thresholds V_{tp}&$V_{tn}$are raised for the MOS transistors, wherein V_{tp} = -3.75V and V_{tn} = 3.75 V. This is accomplished by changing Width / Length(W/L) ratio of the MOS transistors and the corresponding multiplier factor 'M'.When input level is 2.5 V, both pMOS and nMOS transistors and the output nodes will be 2.5V due to the connected auxiliary supply. Obviously, on the resistor there will be a current of 2.5 V/R drawing out of the auxiliary supply if the node value is 0 V, and a current of 2.5 V/R injecting into the auxiliary supply if the node value is 5 V.

3.1.2 Simulation Results and Perfromance Analysis

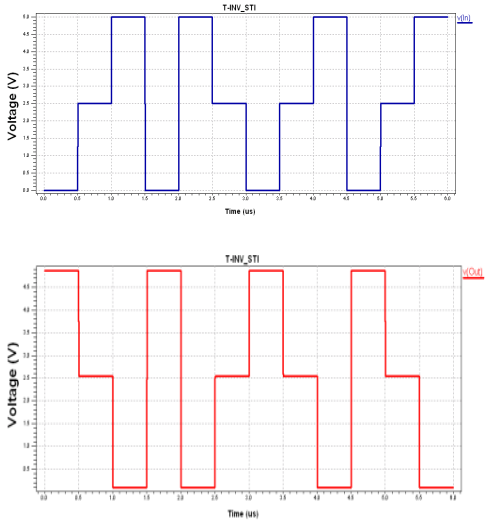
Tanner Tool with its prominent subset, S-Edit, L-Edit, T-Spice and W-Edit are used to derive the various device parameters and further verify the functionality of the gates. The layout is designed using L-edit as depicted in figure 3.1(b). Both, the layout and the schematic of the STI are independently verified using T-spice and W edit.Figure 3.1(c) illustrates the simulation results of STI, verified for all the combinations of the input.



(a)



(b)



(c)

Figure 3.1 Results of TNOT gate (STI gate) (a) schematic (b) layout (c) simulation results

Other universal gates, T-NAND and T-NOR have also been implemented using akin approach. Figure 3.2 indicates the schematic, layout and simulation results of the T-NAND.

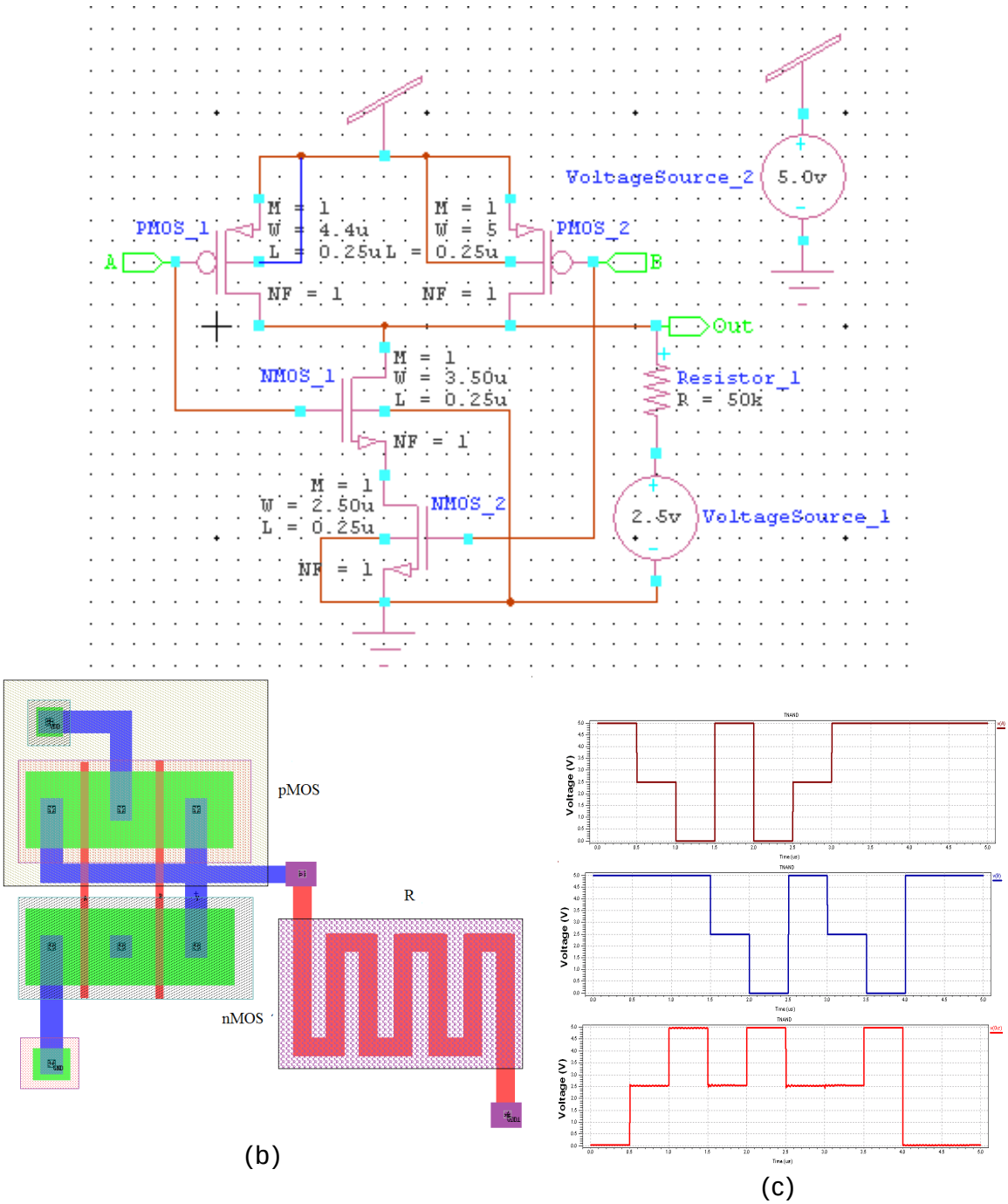


Figure 3.2: Results of TNAND gate (a) schematic (b) layout (c) simulation results

Encouraging results is obtained for T-NOR gate as well. Additional performance analysis of the designed basic gates has been carried out in terms of calculating the rise time and fall time during all the logic transitions. Table 3.1 summarizes the achieved results. The

average dissipated power across the resistor and the MOS transistors is also obtained tabularized in table 3.2.

3.1.3 Discussion on MOSFET based approach

The gates in the original binary logic diagram of the circuit are conceptually transformed into corresponding ternary ones using the injected voltage method [49]. Voltage values for the ternary logic levels were tested for STI, ST-NAND and ST-NOR. The same procedure can be easily extended to design positive and negative ternary logic gates by adjusting the auxiliary supply voltage at 0V and -2.5 V respectively. The choice of the resistance value greatly affects the voltage levels at the output of the T-gates.

Table 3.1: Rise time and fall time of ternary gates

Parameter	**Logic level**	**TNOT**	**TNAND**	**TNOR**
Rise Time	0 to 1	0.74 ns	2.32 ns	2.02 ns
Rise Time	1 to 2	0.74 ns	1.47 ns	1.38 ns
Rise Time	0 to 2	1.69 ns	0.50 us	0.50 us
Fall Time	2 to 0	0.50 us	2.50 us	1.62 ns
Fall Time	2 to 1	1.58 ns	2.10 ns	0.71 ns
Fall Time	1 to 0	1.43 ns	0.73 ns	0.71 ns

Table 3.2: Power dissipation across MOS transistor and resistor

Average Power	TNOT	TNAND	TNOR
MOS Transistors	0.289 µW	1.216 µW	75.62 µW
Resistor	0.378 mW	3.103 µW	98.77 µW

This research examines the performance of designed T gates to estimate the suitable value of resistance. Encouraging results are obtained with R= 15 KΩ in case of STI whereas ST-NAND and ST-NOR give best results with R=50 KΩ. The value of R thus varies with the design. W/L ratio is another important parameter that has a significant impact on the design of the T-gates. This ratio affects the threshold voltage of the MOS transistors. In this design, W/L ratio is suitably maintained to achieve desired voltage values at the output. However, the CMOS based design approach has few major limitations. Use of additional power supply in the CMOS based design to achieve the intermediate voltage level is the major drawback of the design. This will obviously lead to increase in the power plane or power bus in the multilayer PCB. Additionally, use of passive components leads to significant increase in the on-chip area and also increases the power dissipation.

These limitations of the CMOS based approach demand further research to explore additional switching devices for the realization of the ternary logic circuits.

3.2 MIFG Based Design Binary Gates

With the increasing demand for smaller and faster products, there is an ongoing trend in fabrication process towards smaller transistors. In the quest to achieve low-voltage and low-power, various techniques have evolved in due course of time and MIFGMOS transistor technique is one amongst them [13]. MIFG has been detailed in section 2.2. Due to the special characteristics namely, tunability and controllability of the MIFGMOS transistor, its application in both analog and digital circuits has been very wide. This research explores the usability of MIFG for the realization of the ternary circuits.

Binary gates play a crucial role in building efficient ternary combinational and sequential circuits. Further sections of this chapter will make this fact evident. This research therefore initially focused on building MIFG based binary gates.

3.2.1 Binary Inverter using MIFG-MOSFET

A MIFG-MOSFET Inverter with three floating gate inputs has been simulated using T-Spice and W-Edit of Tanner EDA. The input capacitors are C_1, C_2 and C_3. Capacitors C_1 and C_3 are connected permanently to VDD and VSS, respectively. A square wave from 0 to 1.8V DC is applied to input capacitor C_2. The values of C_1, C_2 and C_3 were fixed at 1fF each. By connecting C_1 to V_{DD} and C_3 to Ground (GND), we were able to adjust the switching voltage of the transistors by the equation 3.1.

$$\frac{V_1C_1+V_2C_2\ldots\ldots\ldots V_nC_n}{C_1+C_2\ldots\ldots\ldots C_n+C_0} > V_{th} \ldots\ldots 3.1$$

This has been verified in the simulation plot of transfer characteristics.

All the resistors are high valued resistors (10^{12} ohms) connected in parallel across input capacitors because during simulation to avoid DC convergence.The schematic and input and output waveforms of binary inverter is shown in figure 3.3 (a) and (b) respectively.

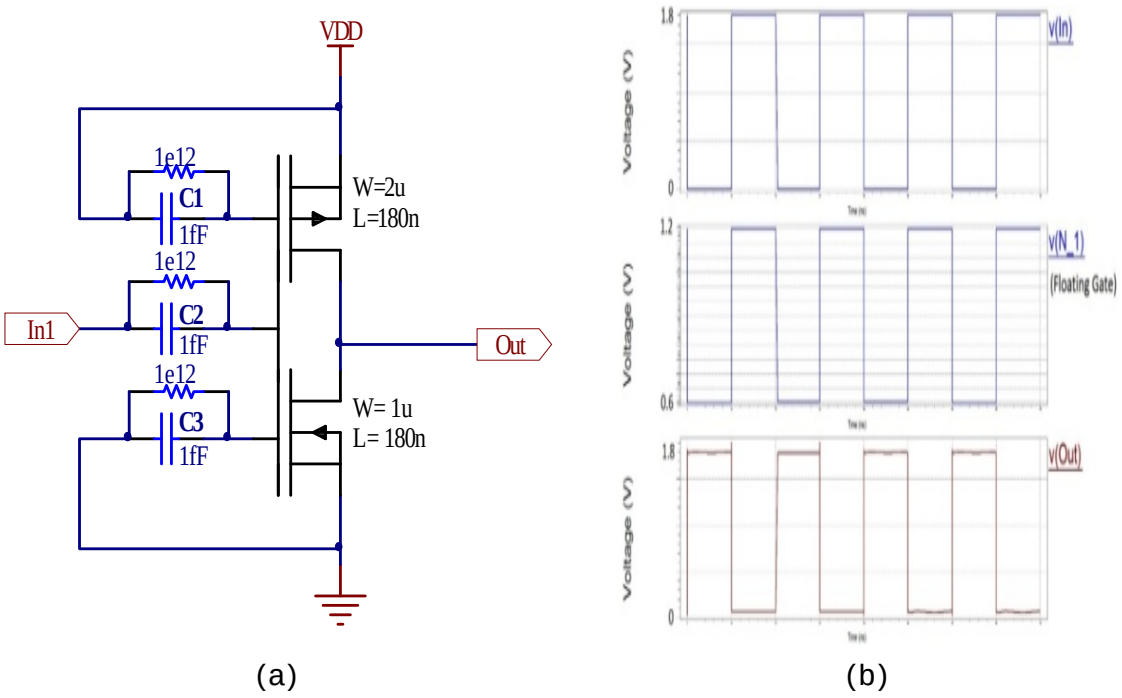


Figure 3.3: (a) MIFG-MOSFET Based Inverter (b) Inverter Input Output waveform

3.2.2 Binary NAND using MIFG-MOSFET

Design of MIFG based binary NAND demands a modification in the circuit designed for binary inverter. In two inputs MIFG-MOSFET NAND, Capacitors C_1 and C_2 act as coupling capacitors for input signals V_1 and V_2, respectively. Capacitor C_3 is permanently connected to V_{SS}. The values of C_1, C_2 and C_3 were fixed at 1fF each. Connecting C_3 to GND, provides a flexibility of adjusting the switching/threshold voltage of the transistors to less than 1.2V. As per the truth table of the binary NAND, both the transistors must switch only when both inputs to the floating gate are at logic high i.e. state '1', i.e. 1.8V. When both inputs are high, the floating gate voltage, calculated by the weighted sum of input signals, is 1.2V.

Considering rest of the input combinations, the floating gate voltage is less than or equal to 1.2V. Thus the switching voltage is adjusted around 0.9V, which ensures the functionality of the binary

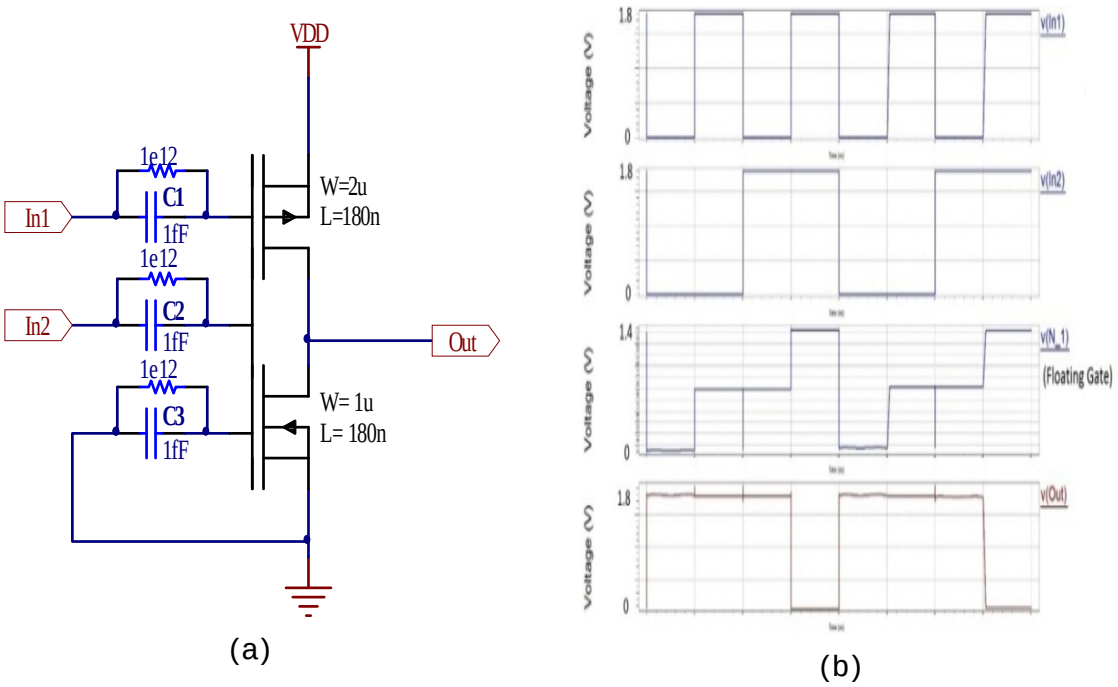


Figure 3.4: (a) MIFG-MOSFET Based NAND Gate (b) NAND Gate input and outputWaveforms

NAND. Figure 3.4(a) depicts the MIFG based binary NAND gate and Figure 3.4(b) represents the input and the output waveforms.

3.2.3 Binary NOR using MIFG-MOSFET

To obtain the functionality of the binary NOR , the Capacitor C_1 is permanently connected to V_{DD}. The coupling capacitors C_2 and C_3 are connected to the input signals V_1 and V_2, respectively. The values of C_1, C_2 and C_3 were fixed at 1fF each. The bias voltages, V_{DD} and V_{SS} are 1.8 V and 0 V, respectively. By connecting C_1 to V_{DD}, it is possible to adjust the switching voltage of the transistors to less than 1.8V. When both inputs are low, the floating gate voltage, calculated by the weighted sum of input signals, is 0V. For all other input combinations, the floating gate voltage is less than 1.8V. Figure 3.5(a) depicts the MIFG based binary NOR gate and Figure 3.5(b) represents the input and the output waveforms. The designed gates are further rigorously analyzed to calculate the Power Delay Product (PDP) at various

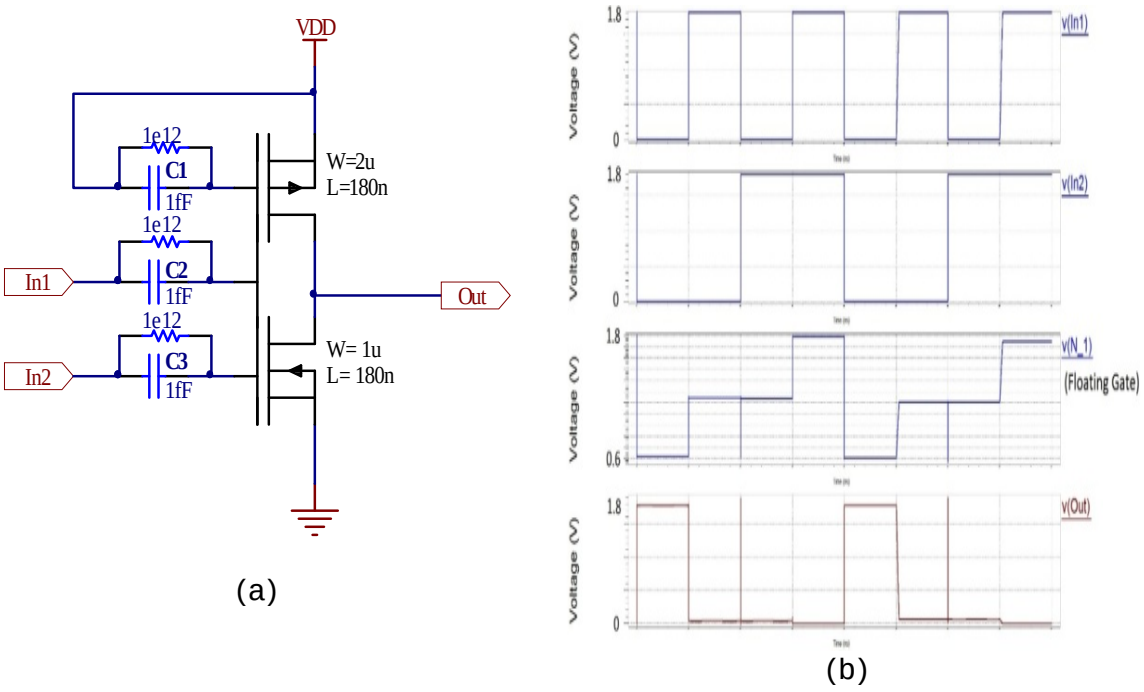


Figure 3.5: (a) MIFG-MOSFET Based NOR Gate (180nm) (b) NOR Gate input and output Waveforms

frequencies, ranging from 500 KHz to 5 MHz and at various loads 1pF to 10 pF. As expected, the PDP increases with increase in load and the designed MIFG based gates deliver promising performance.

3.2.4 Discussions On MIFG based Binary Gates

MIFG has proved to be an intelligent choice for the realization of the binary gates. The designed binary NOT, NAND and NOR gates can be further used to implement the AND, OR, EXOR and XNOR gates. PDP of MIFG-MOSFET gates are acceptable and it not only ensures good functionality but good improvement in the performance parameters is also obtained. Moreover, substantial reduction in the total number of transistors in the design was found to be more than 50%. MIFG based binary gates play a crucial role in efficient realization of the ternary circuits.

3.3 MIFG Based Design of Ternary Gates

The ternary gates are the fundamental building blocks of a ternary processor. MIFG based approach has been devised to extend its suitability for realization of ternary gates. Ternary basic and universal gates, TNOT, TNAND, TNOR, TAND, TOR, TXOR and TXNOR are designed and simulated to validate its functionality and analysis the performance.

3.3.1 Research Methodology

A novel hybrid approach, i.e. a combination of MIFGMOS transistor and conventional MOS transistors is used to design the ternary logic gates. Generally, when designing MIFGMOS transistor based circuits, the conventional MOS may be replaced by MIFGMOS transistor, i.enMOS and pMOS may be replaced by nMIFGMOS transistors and pMIFGMOS transistor respectively. In binary digital circuits such a replacement is expected to deliver the required functionality of the gates. The universal binary logic gates, i.e. NAND and NOR gates have a series and a parallel combination of conventional MOSFETS. Figure 3.6(a) shows a conventional Binary NOR gate. All the MOSFETS can be easily replaced with MIFGMOS transistor making them completely ON or OFF and finally, obtain only two logic states at the output namely logic ‘0’ and ‘1’. Binary gates can therefore be designed using a pure combination of only MIFGMOS transistor as shown in Figure 3.6(b). However, when designing ternary gates three levels must be obtained at the output. The transistors used in the designed circuit must necessarily operate in ON, OFF and intermediate state depending on the given input combination. Unlike binary, an attempt to replace all the conventional MOS transistors with

MIFGMOS transistor, does not deliver the desired functionality of the ternary gates for all the input combinations. Considering the TNOR gate with the input combination A = B = 1; A = 2, B = 0 and A = 0 and B = 2 , the floating gate voltage V_{fg} in all the three cases remains same but the expected output voltage levels are different.

In MIFGMOS transistor the floating gate voltage V_{fg} is the control voltage that decides operating region of MIFGMOS transistor and thus the output. It is impossible to achieve different output logic level when the V_{fg} remains same for various input combinations. There are similar cases even for TNAND gate. The approach of replacing all the MOSFETs in conventional binary gates with MIFGMOS transistor thus fails for designing ternary gates.

Assuming that the series combination of M1 and M2 in NOR gate is replaced by a single MIFGMOS transistor, having two inputs A and B connected to its floating gate as shown in figure 3.6(c). Considering ternary input combination, where A = 2 and B = 1 or vice versa demands output Y to be at logic '1'. Thus, the MIFGMOS transistor must necessarily operate in intermediate state i.e. strong inversion ohmic state. However, when the input A = 2 and B = 1, the floating gate voltage, V_{fg} is sufficiently high to drive MIFGMOS transistor in strong inversion saturation region and make it fully ON. One of the MOSFETs in the parallel arm having logic '2' at its input is also fully ON and thus shorts the V_{DD} to ground. In such a situation the output Y will obviously be pulled down to 0V. This design therefore completely abolishes the occurrence of intermediate state (level '1'), at the output of the ternary gates. It is necessary to restrict the MIFGMOS transistor to strong inversion ohmic region and make it behave like resistor so as to obtain the output as logic '1'. The approach of replacing series combination of MOSFETs with MIFGMOS transistor is highly undesired

from ternary prospective.

Thus when designing the MIFGMOS transistor based ternary logic gates, a hybrid approach comprising of MIFGMOS transistor and conventional MOSFET is inevitable. MOSFETs in the series combinationof NAND and NOR gates must necessarily be retained and the use of MIFGMOS transistor must be exploited in the parallel combination in the circuits as clearly indicated in figure 3.6(d). The ternary gates designed using this approach is detailed in the next section.

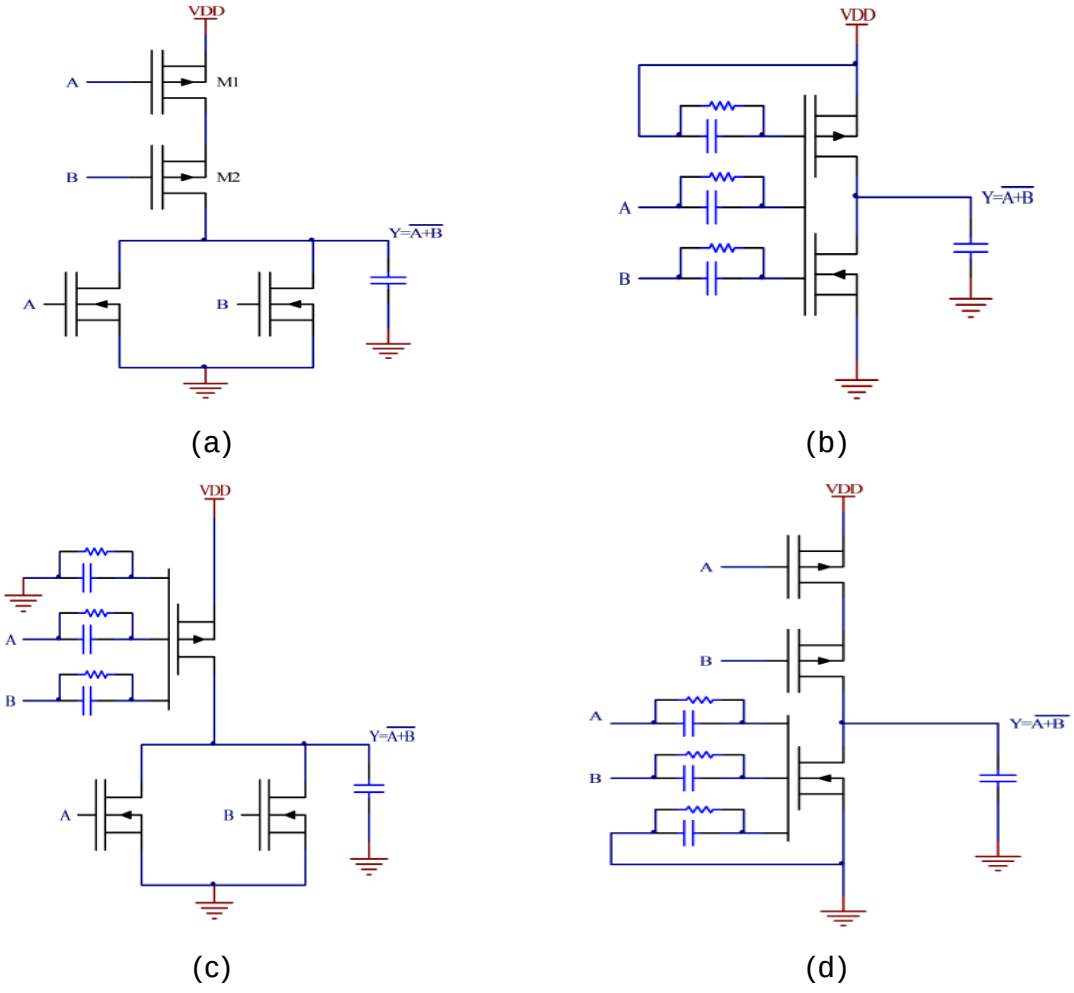


Figure 3.6: (a) Conventional NOR (b) All MOSFETs are replaced by MIFGMOS transistor (c) The series combination of pMOSFETs is replaced by single pMIFGMOS

transistor (d) The parallel combination of nMOSFETs is replaced by single nMIFGMOS transistor

3.3.2 Simulation Results

The structurally developed MIFGMOS transistor must be validated for its functionality and the performance parameters must be analysed using simulators like TSPICE**.** The model parameters for MIFGMOS transistor are not readily available in TSPICE; hence standard MOS models are used to simulate these structures. The electrical components are added to the standard MOS models to emulate the MIFGMOS transistor behaviour. The equivalent circuit of MIFGMOS transistor contains various capacitors. When this circuit is simulated using TSPICE, the problem of floating nodes arises, as a result the simulations fail to converge. As TSPICE cannot accept floating nodes having no dc path to ground, it is necessary to bypass each capacitor with a resistor. The simulation results of the designed gates are detailed below:

(i) Ternary Inverter

As already detailed in section 2.1.3, the Yoeli-Rosinfeld algebra defines three basic ternary elements, the Standard Ternary Inverter (STI), Positive Ternary Inverter (PTI) & Negative Ternary Inverter (NTI) such that,

$$STI = \overline{X^i} = 2 - X$$

$$PTI, NTI = \overline{X^i} = \begin{cases} i \rightarrow X \neq i \\ 2 - i \rightarrow X = i \end{cases} \qquad \text{.....3.2}$$

Where ‘i’ take the value of ‘2’ for PTI & ‘0’ for NTI inverter.

Table 3.3: Truth table of STI, PTI & NTI

A	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table 3.4: Model simulation parameters and node voltages of the designed MIFGMOS transistor based STI circuit

Input 'A'	M1 pMIFG (W = 16 µm, L = 120 nm) V_t= -0.75 v		M2 nMIFG (W= 8 µm, L = 120 nm) V_t = 0.65 V		O/P 'Y'	Ternary logic level
	V_{fg}	V_{gs1}	V_{fg}	V_{gs2}		
0 (0V)	0V	-5V	0	0	5V	2
1 (2.5V)	2.5V	-2.5V	2.5V	2.5V	2.5V	1
2 (5V)	4.78V	0V	4.78V	4.78V	0V	0

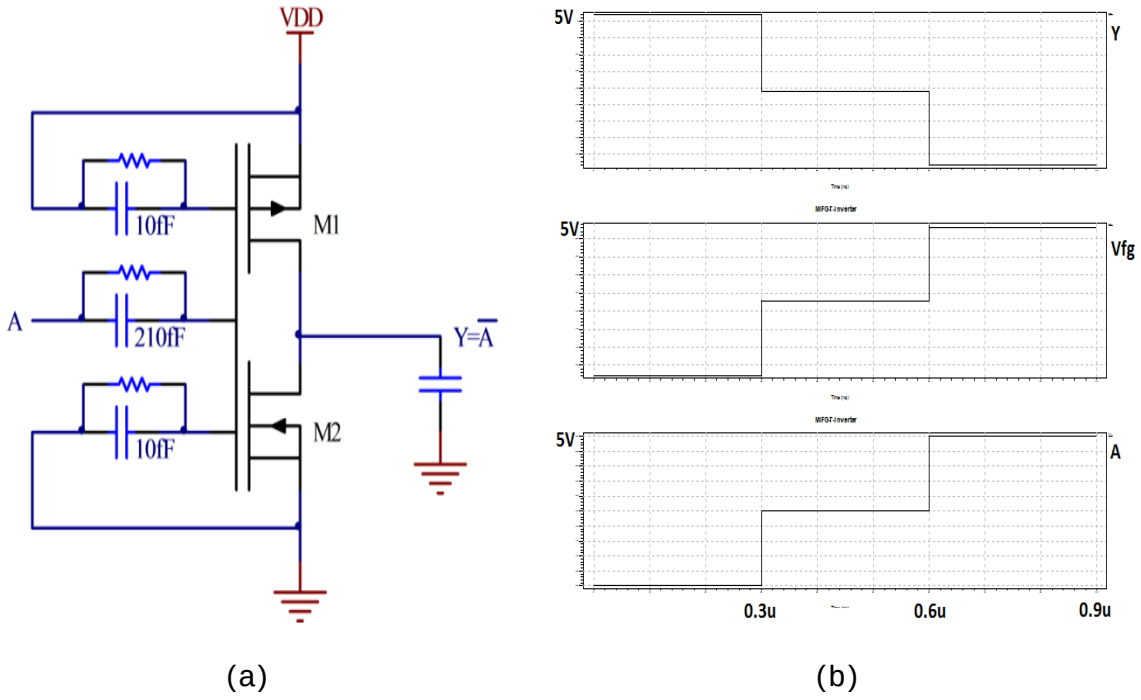
The truth table for the Ternary Inverters, STI, PTI and NTI is given in Table 3.3. Figure 3.7(a) represents the MIFGMOS transistor based STI circuit. The designed circuit is same as the conventional CMOS inverter, except that the transistors have been replaced by MIFGMOS transistor. As depicted in figure 3.7(a) the chosen values of C_1, C_2 and C_3 are 10fF, 210fF and 10fF respectively. Equation number 3.3 of V_{fg} becomes

$$V_{fg} = \left(\frac{C_1 V_1 + C_2 V_2 + C_3 V_3}{C_T} \right) \text{.....3.3}$$

Where $C_T = C_1 + C_2 + C_3$

V_{fg} = Voltage at the floating gate

V_{fg} is common to both the transistors in the designed STI. Table 3.4 details the operational voltages of the MIFGMOS transistor based STI.



(a) (b)

Figure 3.7: (a) MIFGMOS transistor based STI (b) input and output waveform ofSTI

As illustrated, using equation number 3.2 the calculated values of V_{fg} for logic 0, 1 and 2 are 0 V, 2.5 V and 4.78 V. The threshold voltage of the designed gate is -0.75 V and 0.65 V for M1 and M2 respectively.

When the input 'A' is at logic '0', transistor M1 is operating in strong inversion saturation i.e. ON state. However, no inversion layer is formed in transistor M2 thereby forcing it to be in OFF state and making the output Y to be at logic '2'. Similarly when the input 'A' is at logic '2', the V_{fg} is greater than V_{th}which is 0.65, making it operate in strong inversion saturation and thus turning it ON. Transistor M1 is OFF, bringing the output Y, at logic '0', thus inverting the input as per the truth table of STI. Logic '1' at the input A, drives the transistors to

operate in the intermediate state, thus making both of them behave like a resistor. In such situation, the circuit behaves like a voltage divider, producing the output of V_{DD} /2 , i.e. 2.5 V (Logic 1) at the output. figure 3.7(b) illustrates the simulation results of the devised MIFG based STI that conform with the input output conditions described in table 3.4.The effect of W_p/W_n on voltage transfer curve of STI is depicted in figure 3.8.

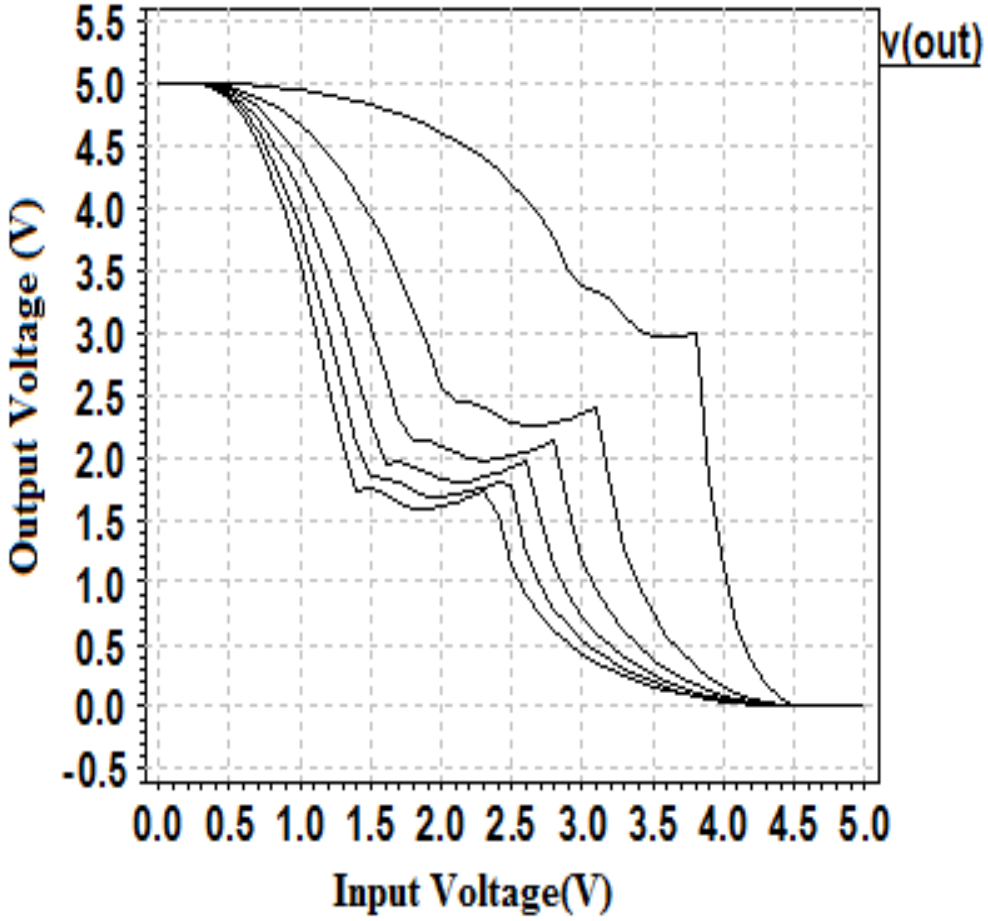


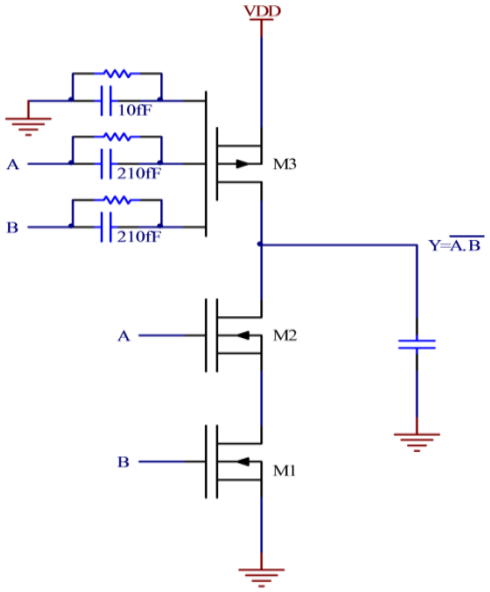
Figure 3.8: VTC curve of STI

(ii) Ternary NAND (TNAND)

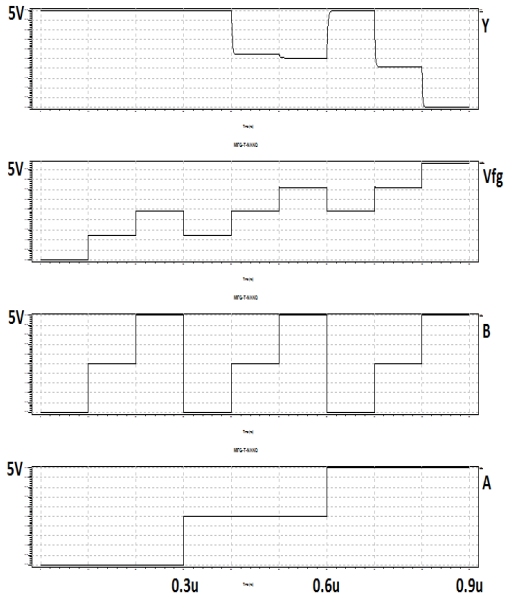
The TNAND gate can be defined as,

$$TNAND = \overline{X_1 \cdot X_2 \cdot ..... \cdot X_n} = Min\,[\overline{X_1, X_2, ... X_n}] \quad ...3.4$$

The sign '.' indicates logical ternary AND operation. The Ternary NAND gate can be configured as STNAND, PTNAND and NTNAND. Table 3.5 represents the truth table of the STNAND gate. Figure 3.9(a) represents the novel MIFG based STNAND circuit. The conventional binary CMOS based NAND circuit is modified by replacing the parallel combination of pMOS by a single pMIFG. The nMOS in the series arm of the binary NAND are retained in the design of the ternary gates. The MIFG based design thus reflects a novel hybrid combination of the circuit elements to achieve the functionality of the ternary STNAND gate.



(a)



(b)

Figure 3.9: (a) Ternary NAND (b) input and output waveform of T-NAND

Table 3.5: Truth table of STNAND

Input	**A**	0	0	0	1	1	1	2	2	2
	B	0	1	2	0	1	2	0	1	2

Output	**Y**	2	2	2	2	1	1	2	1	0

As depicted in figure 3.9(a) the chosen values of C_1, C_2 and $C_3$are 210fF, 210fF and 10fF respectively. The differential voltage between floating gate and the source terminal of MIFG decides the state of operation of pMIFG. The threshold voltage, $V_{th}$of M3 is -0.65V and V_{th} of M2 and M1 is 1.3V and 0.85V respectively. For the different logical states of input A and B the operations of the circuit are discussed below.

When both the inputs A and B of the designed Ternary gate are logic '0', the transistor M3, i.e. pMIFG is completely ON and is operating in the strong inversion saturation. The nMOS in the series arm that receives logic state '0' input is in OFF state thus bringing the output Y at logic '2'.

When both the inputs, A and B are at logic '2' the pMIFG M3 is in OFF state. The nMOS transistors, M1 and M2 are operating in strong inversion saturation. So the output Y is pulled to logic '0'.

When one of the inputs to the ternary STNAND is at logic '1' and if the other input is either at logic '1' or '2', in such a case the output Y is at logic '1'.

When one of the inputs to the ternary STNAND is at logic '0' and if the other input is at logic '2' or logic '1',the output Y is at logic '2'. The transistor M3 operates in strong inversion ohmic region. The nMOSFET having input logic '0' is in cut-off state thereby making the rail to rail Id drop to zero. The sourcing current of pMIFGMOS transistor is in such a situation which is less as compared to its sourcing current when the output Y is at logic '2'.

In all the above cases, the pMIFG operates in strong inversion ohmic region. When one of the inputs is at logic '2', the corresponding

nMOSFET is fully ON and driven into strong inversion saturation region. The remaining nMOSFET and pMIFG operates in strong inversion ohmic region and forms a voltage divider circuit to deliver output at logic '1'.

The nMOSFET having input logic '0' is in cut-off state thereby making the rail to rail I_d drop to zero. The sourcing current of pMIFGMOS transistor in such a situation is less as compared to its sourcing current when the output Y is at logic '2'.

The floating gate voltage, V_{fg} when inputs A = 0 ,B = 2 and A=B=1, is same for both the cases but the expected logic level at the output is different ,Y=2 and Y= 1 respectively. The novel hybrid approach of using a combination of both the devices, MIFG and MOSFET has addressed the issue and has delivered good results for all the combination of inputs.

The simulation results for all the input combinations and the voltage levels Y, depicted in fig 3.9(b) confirms the functionality of the designed gates. The designed gates are further rigorously analyzed to calculate the PDP at various frequencies ranging from 500 KHz to 5 MHz and at various loads from 1pF to 10 pF. As expected, the PDP increases with increase in load and the designed MIFG based gates deliver promising performance

(iii) TERNARY NOR (TNOR)

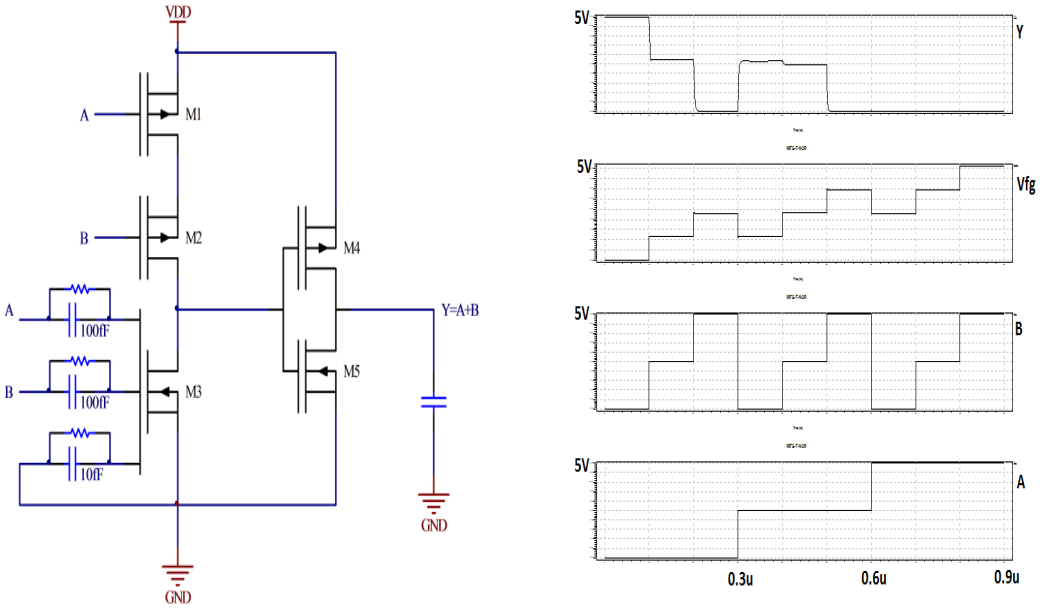
Ternary NOR has an output that is a compliment of OR function i.e.

$$TNOR = \overline{X_1 + X_2 + ... + X_n} = Max\,\overline{[X_1, X_2 ... X_n]} \qquad .....3.5$$

The sign '+' indicates logical ternary OR operation. The Ternary NOR gate can be configured as STNOR, PTNAND and NTNOR. Table 3.6 represents the truth table of the TNOR gate. Figure 3.10(a) represents the novel MIFG based STNOR circuit designed in this research. The

conventional binary CMOS based NOR circuit is modified by replacing the parallel combination of nMOS by a single nMIFG, M3. The two pMOS in the series arm of the conventional binary NOR are retained in the design of the ternary gates as M1 and M2. The devised novel MIFG based design thus reflects a novel hybrid combination of the circuit elements to achieve the functionality of the ternary STNAND gate.

As depicted in Figure 3.10(a) the chosen values of C_1, C_2 and C_3 are 100fF, 100fF and 10fF respectively. The differential voltage between floating gate and the source terminal of MIFG decides the state of operation of nMIFG. The threshold voltage, $V_{th}$of M3 is 0.8V and V_{th} of both, M2 and M1 is -0.8V.



(a) (b)

Figure 3.10: (a) TNOR (b) input and output waveform of T-NOR(b) illustrates the simulation results for all the input combinations.

Table 3.6: Truth Table of TNOR Gate

Input	**A**	0	0	0	1	1	1	2	2	2
	B	0	1	2	0	1	2	0	1	2

Output	**Y**	2	1	0	1	1	0	0	0	0

For the various logical states of input A and B the operations of the circuit are discussed. When both the inputs are '0', M3 is OFF and both M1 and M2 are ON and operates in strong inversion saturation, providing path to V_{DD}. Logic level of '2' is obtained at the output Y.When one of the inputs, A or B is at logic '1' and the other input is either '0' or '1' , the transistor M3 is at strong inversion ohmic region. The transistor M1 or M2 receiving logic level '1' at its input operates in strong inversion ohmic region. The MOSFET receiving logic '0' is completely ON and operates in strong inversion saturation region. The circuit behaves as voltage divider and produces an output of $V_{DD}/2$ i.e. logic '1' at Y.

The floating gate voltage obtained because of above combinations is different but the expected output for all is Y= 0 for all of them. When one of the inputs is at logic '2', the pMIFG is driven into strong inversion saturation region and pMOSFETs that receives logic '2' at its input is in cut-off state, thereby disconnecting the path from V_{DD} to output and thus forcing Y to be at logic '0'.

In above three cases, the floating gate voltage, V_{fg}, obtained due to these input combinations is same but the expected logic level at the output is different. When both the inputs A=B=1 , all the transistors operate in saturation inversion ohmic region and function as voltage divider to deliver an output of logic '1'. On the contrary, in remaining two combinations of inputs, M3 operates in strong inversion ohmic region and as already discussed, the output Y, is pulled down to logic '0' because one of the pMOSFET operates in cut-off region. The sinking current of nMIFGMOS transistor is in such a situation which is less as compared to its sinking current when the output Y is at logic '0'. This condition decides the maximum fan out for the designed

TNOR gate. The voltage levels at V_{fg} are also depicted in the figure 3.10(b). The output voltage Y confirms the functionality of the designed gates.

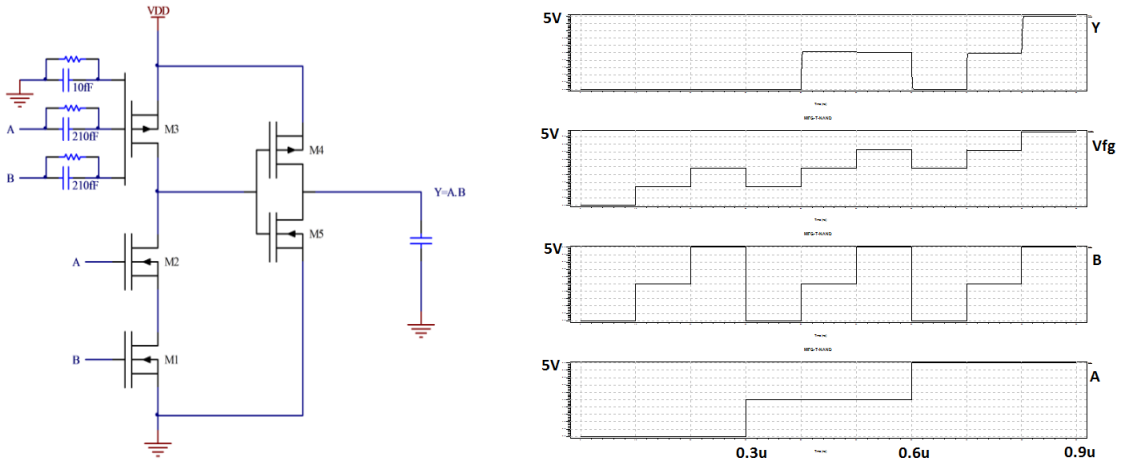
Table 3.7: Truth table of the Ternary gates

A	B	TNAND	TAND	TNOR	TOR	TXOR	TXNOR
0	0	2	0	2	0	0	2
0	1	2	0	1	1	1	1
0	2	2	0	0	2	2	0
1	0	2	0	1	1	1	1
1	1	1	1	1	1	1	1
1	2	1	1	0	2	1	1
2	0	2	0	0	2	2	0
2	1	1	1	0	2	1	1
2	2	0	2	0	2	0	2

(iv) Ternary AND and Ternary OR (TAND and TOR)

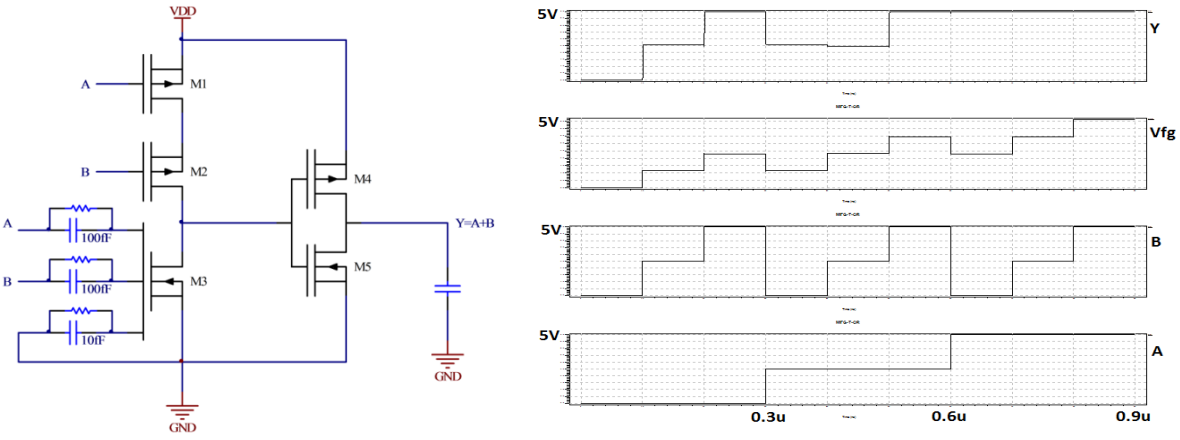
TAND gate is designed by inverting the outputs of ternary NAND using STI. Table 3.7 indicates the truth table of TAND. The circuit diagram of the designed TAND is illustrated in Figure 3.11(a). The simulated input-output waveform of the TAND is shown in Figure 3.11(b).

Similar to TAND, TOR gate is designed by inverting the output of TNOR gate. The circuit diagram of the designed TOR is illustrated in figure 3.12(a). The simulated input-output waveform of the TOR is shown in figure 3.12(b).



(a) (b)

Figure 3.11: (a) Ternary AND (b) input and output waveform of TOR



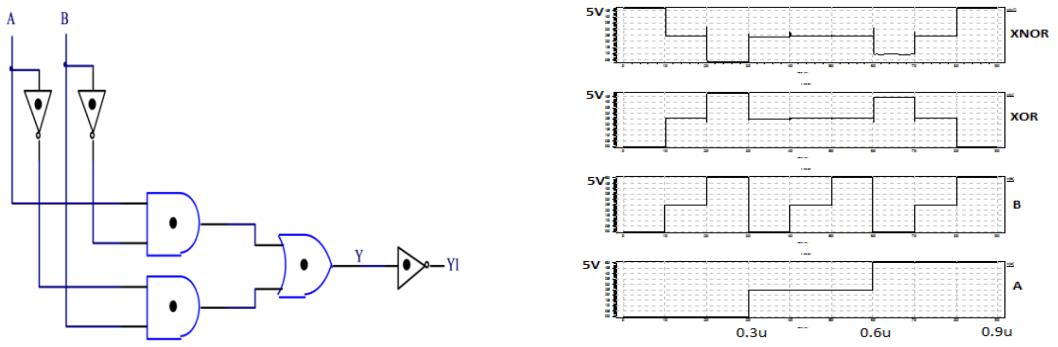
(a)

(b)

Figure 3.12: (a) Ternary OR (b) input and output waveform of TOR

(v) Ternary XOR AND Ternary XNOR (TXOR and TXNOR)

TXOR and TXNOR functions can be implemented by combining the STI, TAND, and TOR gates as indicated in figure 3.13(a). The output of TXOR, Y is further complemented to obtain the output of TXNOR, Y1. The truth table of both the gates is represented in table 3.7. The simulated input-output waveform of the ternary XOR and XNOR gate is shown in figure 3.13(b).



(a) (b)

Figure 3.13: (a) Ternary EXOR and EXNOR (b) input and output waveform of TEXOR and TEXNOR

3.3.3 Discussion on MIFG based approach for ternary gates

This research presents a novel hybrid approach based on MIFGMOS technology for the realization of the ternary gates. The designs of two input TNAND and TNOR gates are detailed. The designed TNAND and TNOR gates along with MIFGMOS transistor based T-inverter is further used to design TAND, TOR, TXOR and TXNOR gates. An extensive simulation of all the designed gates is carried out using TSPICE circuit simulator. The results demonstrate expected functionality of the novel hybrid gates and an additional improvement in the performance parameters is also achieved. The designed gates are further rigorously analyzed to calculate the PDP at various frequencies ranging from 500 KHz to 5 MHz and at various loads from 1pF to 10 pF. As expected, the PDP increases with increase in load and for a specific load, the PDP remains constant in spite of large variations in frequency. The designed MIFG based gates deliver promising performance. The earlier reported CMOS technique for the implementation of ternary gates uses an additional power supply and passive components to obtain the intermediate state i.e. logic state '1' [6, 50]. This is because, in such circuits CMOS operates only in ON and OFF states. The devised novel approach however eliminates the need

of additional power supply and components to achieve the intermediate state. The weighted sum of the input voltages at floating gate provides the flexibility to drive the circuit in ON, OFF and intermediate state. This is significant improvement as compared to the earlier CMOS designs [6, 50].

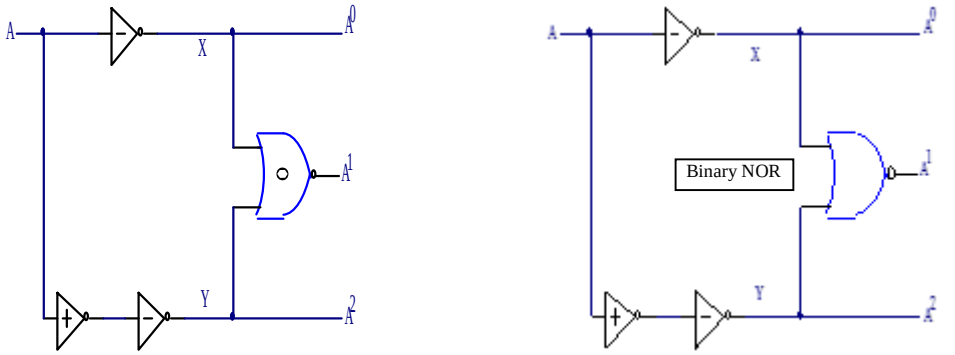
3.4 Ternary Decoder

In ternary logic a literal '*A*' must be uniquely represented as A^i where *i* takes value , '0', '1' and '2'*i.e*A^0, A^1 or A^2. The superscripts in different input represent the state on the input such as A^0 represents the low state, A^1 represents the intermediate state, and A^2 represents the high state. A^0, A^1 andA^2 are the unary outputs obtained from the ternary decoder. In realization of ternary combinational circuits a ternary decoder is therefore necessary which generates unary functions A^0, A^1 or A^2. In other words, equations for the binary logic circuits can be easily generated because the SoP terms represent the logic state '1' by default. However in ternary logic, both the terms, corresponding to output i.e. V_{DD} (logic state '2') and V_{DD} /2 (logic state '1'), must be necessarily considered and explicitly indicated when representing the equations of ternary circuits. Consider, the first term of equation 3.6 which by default indicates the output logic state '2' and the second term signifies the output logic state '1'.

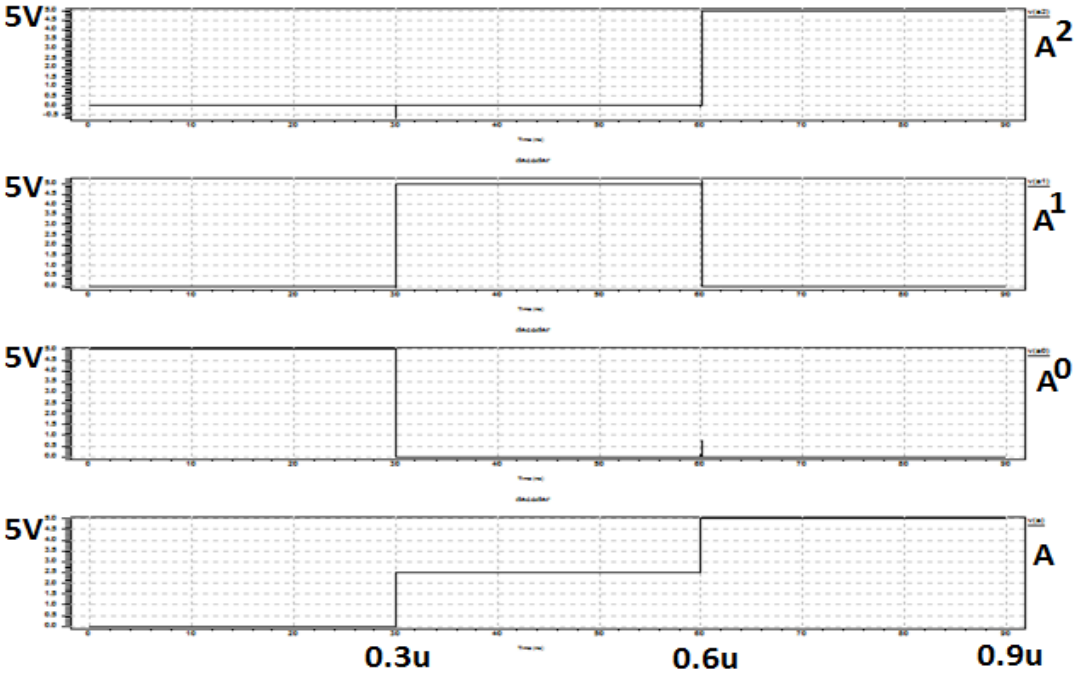
$$Y = (A^0 B^1) + 1.(A^1 B^2) \quad \text{.....3.6}$$

It is thus imperative that for a given ternary input *A*, all the possible literals A^o , A^1 *and* A^2 must have unary values. A decoder which provides this functionality is therefore necessary when realizing the ternary gates. Ternary decoder is one-input, three-output combinational circuit that generates unary function for an input *A*. A ternary decoder consists of a PTI gate, two NTI gates and a TNOR gate

as shown in figure 3.14(a).



(a) (b)



(c)

Figure 3.14: (a) Conventional ternary decoder using ternary TNOR gate using STI and PTI (b) Modified ternary decoder using binary NOR gate (c) The input-output waveforms of the modified ternary decoder.

Table 3.8: Truth table of the ternary decoder

A	X	Y	A^0	A^1	A^2
0	**2**	**0**	2	**0**	0
1	**0**	**0**	0	**2**	0
2	**0**	**2**	0	**0**	2

3.4.1 Research Methodology for designing modified Ternary decoder

A hybrid approach based on MIFGMOS transistor and conventional MOS transistor is used to implement the TNOR gate in the ternary decoder. Table 3.8 details the truth table of the decoder. A keen observation of the truth table stimulates further improvement in the design of ternary decoder. As clearly indicated the inputs '*X*' and '*Y*' of the TNOR and its output 'A^1'are either '0' or '2' for any ternary input '*A*'. The TNOR gate in the conventional ternary decoder can therefore be replaced by binary NOR gate as indicated in figure 3.14(b). MIFGMOS transistor based binary NOR gate is used in the modified ternary decoder and to achieve reduction in the number of circuit elements. The simulation results of modified ternary decoder also depict in figure 3.14(c).

3.4.2 Discussion on MIFG based modified Ternary decoder

The modified MIFGMOS transistor based ternary decoder achieves reduction in circuit element count and requires only 9 circuit gates as compared to the reported 20 circuit elements using CNTFET [1] and 13 circuit elements using QDGFET [13] based approaches. The comparison of the circuit elements used in the ternary decoder highlight the benefits neither of the using binary NOR in the design of modified ternary decoder. A further reduction to only 8 circuit elements is achieved using MIFG based binary gate in the modified

ternary decoder.

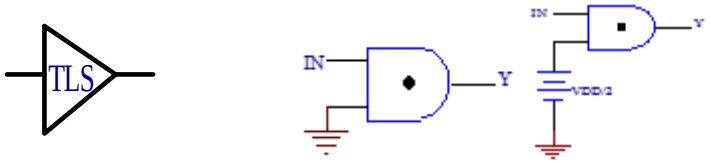
3.5 Design of Novel Ternary Level Shifter (TLS)

The researchers have proposed two different ternary logic systems namely, balanced and unbalanced logic system for realization of the ternary circuits. Balanced system uses $-V_{DD}$ for logic 0, 0V for logic 1 and + V_{DD} for logic 2 and unbalanced system uses 0V for logic 0, V_{DD} / 2 for logic 1 and, V_{DD} for logic 2. Irrespective of the balanced or unbalanced systems, a TLS which is also called as T-buffer, it is a vital component in the realization of ternary digital circuit. The symbol representing the device is shown in figure 3.15(a).The logic function of a TLS can be represented as equation 3.7, where $Y_o$is the output of the TLS and *A* is the input.

$$Y_0 = \begin{cases} 1, & if \quad A = 1,2 \\ 0, & if \quad A = 0 \end{cases} \qquad \text{.....3.7}$$

It shifts the higher voltage (logic state '2') to intermediate voltage level (logic state '1'), thusgiving the output of 2.5 V for unbalancedternarysystems or 0V for balancedternary. However, the design of TLS has recievedless attention by the researchers. The reported TLS use a TAND gatewith one of itsinput connected to 2.5 V or 0 V as indicated in figure 3.15(b) [11]. The voltage level of the input 'A' isshifted to intermediate voltage level as represented by output 'Y' of TLS.

The existing level shifters cannot be directly used for ternary combinational circuits. Literature reports use of an AND gate with one input connected to V_{DD} / 2 as a level shifter. An additional power supply and passive components are usually required that function as voltage divider to obtain the required voltage of V_{DD}/ 2.



(a) (b)

Figure 3.15: (a) Symbol of TLS (b) Reported gate work as TLS

This obviously leads to the power consumption issues related to the voltage divider circuit. Moreover there are limitations of the voltage divider to act as precise reference. To overcome these limitations of the reported TLS, this research presents a novel TLS using a hybrid approach combining MIFGMOS and conventional MOS.

3.5.1 Research Methodology for designing TLS and its simulation results

The two most important properties of MIFG are

- *Controllability*: The effective floating gate voltage V_{fg}, of every single MIFGMOS transistor can be controlled separately according to expected operating region.
- *Tunability*: It is a multiple input device and can be designed to be tuned just by adding extra inputs.

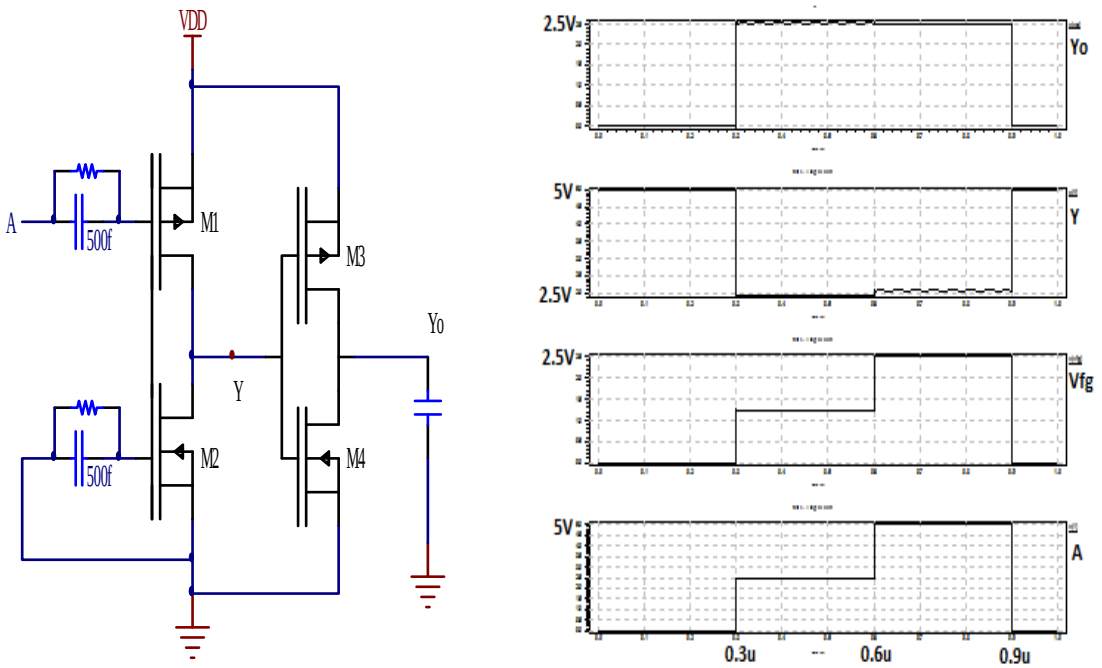
The novel TLS presented in this research exploits the controllability and tunability of the MIFGMOS transistor to achieve an intermediate voltage level and the desired functionality of the level shifter. Moreover the need of passive components and an additional power supply is completely eliminated leading to considerable reduction in the power.

As indicated in figure 3.16(a), the designed TLS is a combination of two stages with the chosen value of the input capacitors, C_1 and C_2 as 500fF each. The first stage, complementary MIFG MOS transistor

M1 and M2 is cascaded with a complementary conventional MOS pair M3, M4. The CMOS pair M3 and M4 behaves as a ternary inverter, complementing the output Y of the first stage.

As per the equation 3.7 the output Y_0 of TLS must be at logic '1' when the input is at logic state '1' or logic state '2'. The input logic when '0' must be retained at the output giving *Y_0= '0'.* When *A is0* ,*$V_{fg}$is 0*results in making *V_{gs}*of M1 switch to -5V. This causes M1 to operate in saturation region. The *V_{gs}* of transistor M2 is zero thereby switching it off. The output of the first stage 'Y' therefore is pulled to logic state '2'. The second stage complements the input 'Y' and drives M3 to cut-off and M4 to saturation region thereby finally delivering an output of 0V as desired. When *A is '1'* or *A is '2'* , the floating gate voltage V_{fg} is sufficiently high to drive both the transistors M1 and M2 to strong inversion ohmicregion and make them behave as voltage divider delivering output of V_{DD} /2 i.e logic state '1' at the output Y_o . This voltage is further complemented by the ternary inverter. The transistor pair M3 and M4 also operate in ohmic region and output logic state '1' is finally obtained at the Y_o. The floating gate voltage *V_{fg}* in the design is adjusted using different fixed input voltages.

Use of an additional input V_2 has provided the flexibility of controlling *V_{fg}* by adjusting the denominator. The differential voltage, *V_{gs}*thus obtained for the input logic states '1' and '2'drives theMIFGMOS transistors in strong inversion ohmic region, pulling output Y to logic state '1' which is further inverted to finally obtain Y_o as '1'. The same output state (logic state '1') can therefore be obtained for two different input logic states '1' and '2'.The designed MIFGMOS transistor based approach, exploiting the controllability and the tunability of MIFG thus makes it possible to achieve the intermediate state of logic '1', without an additional power supply thereby introducing the functionality of the



(a) (b)

Figure 3.16: (a) The novel TLS (b) The input-output waveforms of TLS

TLS. The input output waveforms of the TLS are illustrated in figure 3.16(b).

3.5.2 Discussion on the Novel MIFG based TLS

Design and realization of TLS has received meager attention by researchers. This research presents a novel hybrid approach based on MIFG and conventional MOSFET to design TLS which is extensively simulated to verify its operation. The TLS designed in this research achieves an intermediate voltage level (logic level '1') and the desired functionality. Moreover the need of passive components and an additional power supply is completely eliminated, which automatically leads to considerable reduction in the power, thus addressing major issues reported in the literature.

3.6 MIFG Based Design of Ternary Arithmetic and Logical Unit(TALU)

Arithmetic Logic Unit (ALU) forms an inherent entity of every processor. The designed ternary gates and the binary gates are used to realize a ternary ALU (TALU). The architecture of 1-trit TALU is shown in figure 3.17. The TALU based on ternary gates and combination of both binary and ternary gates has same architecture except the types of gates. The transmission gates and processing modules are the main functioning blocks of TALU.

Ternary decoder is implemented to generate three levels, say A^0, A^1 and A^2 corresponding to ternary input 'A'. The same applies for input 'B' and 'C'. Depending on the input from the Function Selection Logic (FSL), the transmission gates select the corresponding ternary arithmetic or logical combinational circuits. The FSL also simultaneously activates the multiplexer to deliver output of the enabled combinational block at Y_0 and Y_1. The arithmetic blocks namely adder, subtractor and multiplier use two outputs, Y_0 and Y_1, whereas logical functions need only one output Y_0. Since ternary comparator has three outputs, Y_2, Y_3 and Y_4 are depicted as an individual block in figure 3.17.

The functional details of the designed TALU to perform a specific operation corresponding to the combination of the select lines S_0 and S_1 are represented in table 3.9. The devised TALU considers only a few logic blocks which can be easily extended to include more logical operations using additional select lines. The subsequent section describes the MIFGMOS based approach to design the processing blocks of the TALU.

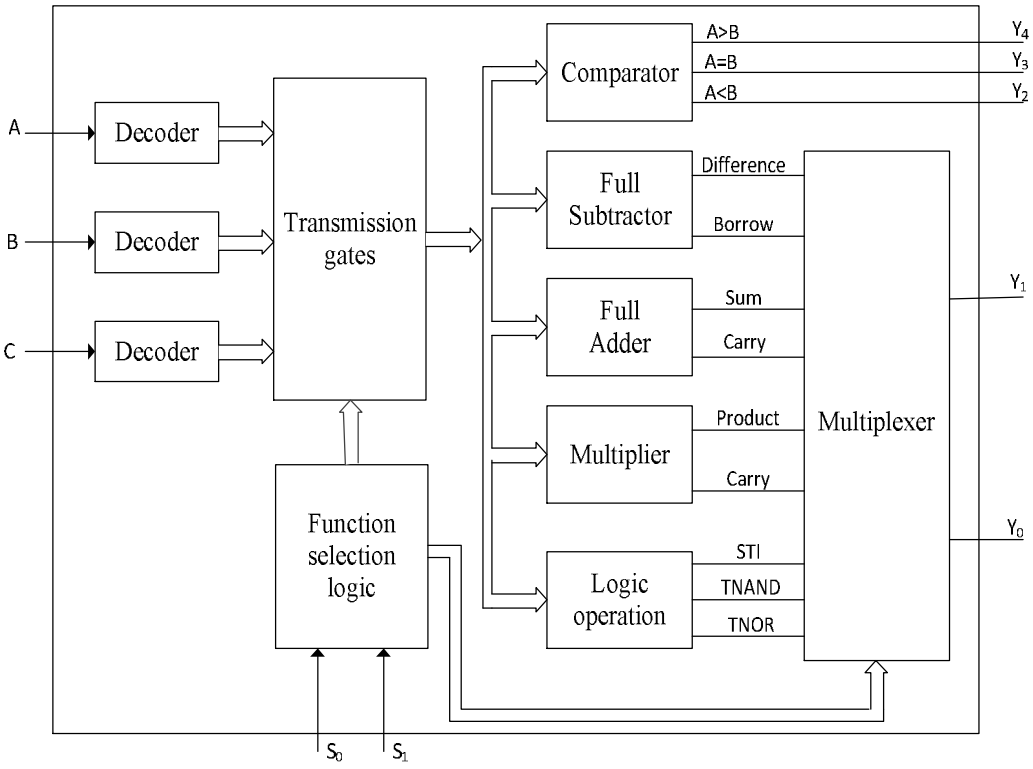


Figure 3.17**:** MIFGMOS transistor based 1- trit TALU

Table 3.9: Function details of the TALU

S_0	S_1	**Operations**
0	**0**	Addition
0	**1**	Subtraction
0	**2**	Multiplication
1	**0**	A=B
1	**1**	A<B
1	**2**	A>B
2	**0**	Inversion
2	**1**	NAND
2	**2**	NOR

3.6.1 Ternary Half Adder (THA)

The Ternary Half Adder (THA) adds two ternary trits and produces two outputs i.e. ternary sum and ternary carry. The Karnaugh Map as indicated in Figure 3.18 is represented using the truth table depicted in table 3.10. The logic equations for the realization of the logic functions, Sum and Carry of the THA are derived. The equation 3.8 and 3.9 are implemented using the ternary decoder, TLS and the ternary gates as illustrated in figure 3.19(a).

Figure 3.18: Kaurnaugh Map of Ternary Half Adder

	Sum output			**Carry output**		
A / B	**0**	**1**	**2**	**0**	**1**	**2**
0		1	2			
1	1	2				1
2	2		1		1	1

The logic equations are:

$$Sum = (A^0B^2 + A^1B^1 + A^2B^0) + 1.(A^0B^1 + A^1B^0 + A^2B^2) \quad \text{.....3.8}$$

$$Carry = 1.(A^1B^2 + A^2B^1 + A^2B^2) \quad \text{.....3.9}$$

As reported in [1], if the ternary and binary logic gates are used to take advantage of their respective merits, performance could be significantly improved because ternary logic is a good candidate for logic circuits while binary logic is a good candidate for fast computing modules. The output of the decoder has only two logic values i.e. ‘2’ and ‘0’, corresponding to logic ‘1’ and ‘0’ in binary logic. Therefore binary gates can be used in a ternary circuit for accomplishing a faster

operation.

Table 3.10: Truth table of Ternary Half Adder

Input		**THA**	
A	**B**	Sum	Carry
0	**0**	0	0
0	**1**	1	0
0	**2**	2	0
1	**0**	1	0
1	**1**	2	0
1	**2**	0	1
2	**0**	2	0
2	**1**	0	1
2	**2**	1	1

A modified THA is shown in figure 3.19(b) designed by replacing the ternary logic gates in the highlighted block by binary logic gates. The MIFGMOS transistor based AND and OR binary logic gates are used in the improved THA. It must be noted that this replacement delivers the same functionality but achieves further reduction in the MOSFET count as compared to half adder designed using only ternary gates. The simulation result of the designed MIFGMOS based half adder is depicted in figure 3.19(c). The input output waveforms confirm the functionality of the MIFGMOS based half adder. The designed MIFGMOS THA are further analyzed in terms of the transient response and compared with the state of art methods.

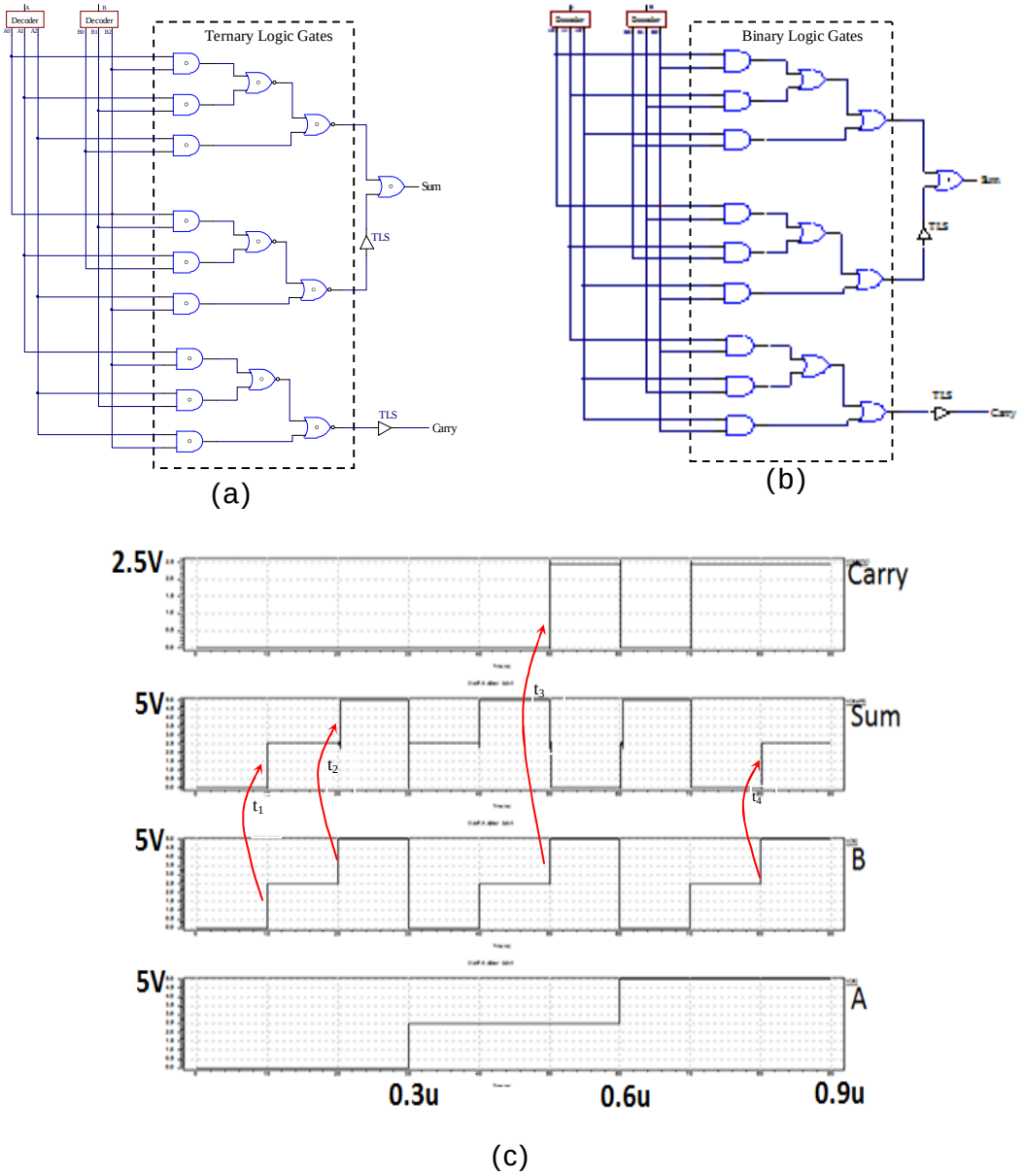


Figure 3.19: (a) Logic diagram of the THA using ternary gates (b) Logic diagram of the THA using binary gates (c) The input output waveforms of the THA using binary

3.6.2 Ternary Full Adder (TFA)

A 1-trit Ternary Full Adder (TFA) adds three 1-trit numbers. The operands *A* and *B* and the $C_{in}$from the previous stage or past addition are added to produce a 2-trit result, Sum and C_{out}, as represented in truth table 3.11. The logical equation 3.10 and 3.11 can be used for the gate level realization of the TFA. It is evident that such a

realization would need a total of 43 ternary gates. The same functionality of the TFA, but with comparatively less number of circuit elements can also be achieved using THA based design.

$$Sum = (B^0C^2 + B^1C^1 + B^2C^0)(A^0 + 1.A^2) + (B^0C^1 + B^1C^0 + B^2C^2)(A^1 + 1.A^0) + (B^1C^2 + B^0C^0 + B^2C^1)(A^2 + 1.A^1)$$

.....3.10

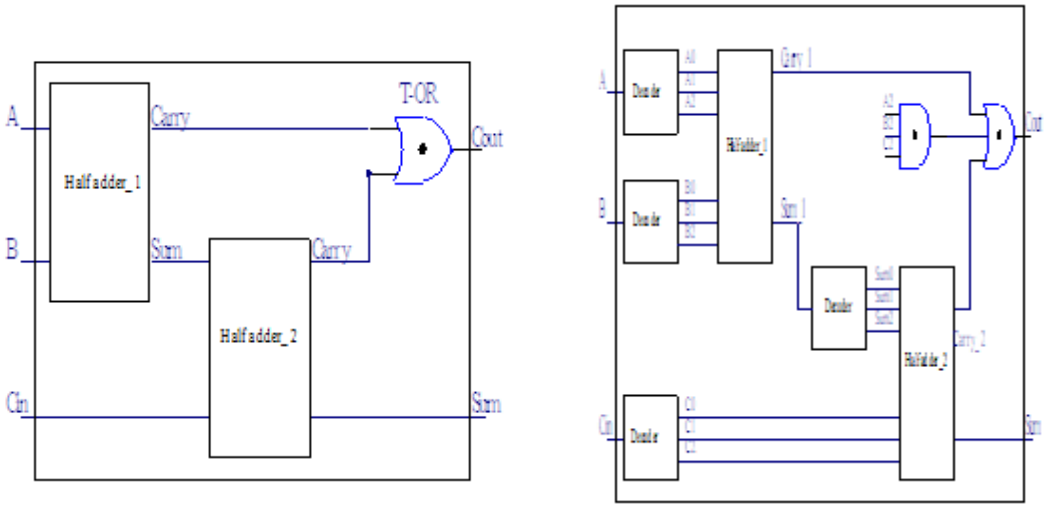
$$Carry = A^2B^2C^2 + 1.(A^0B^{12}C^2 + A^0B^2C^{12} + A^1C^2 + A^1B^{12}C^1 + A^1B^2 + A^2B^{12} + A^2C^{12})$$

.....3.11

Table 3.11: Truth table of Ternary Full Adder

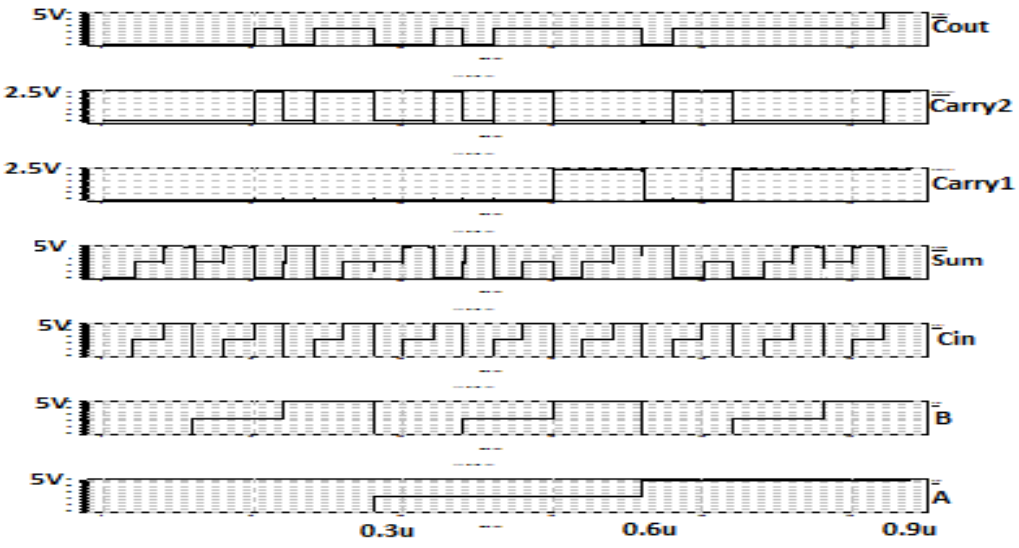
Inputs			**TFA**	
A	**B**	C_{in}/Borrow	C_{out}	Sum
0	**0**	0	0	0
0	**0**	1	0	1
0	**0**	2	0	2
0	**1**	0	0	1
0	**1**	1	0	2
0	**1**	2	1	0
0	**2**	0	0	2
0	**2**	1	1	0
0	**2**	2	1	1
1	**0**	0	0	1
1	**0**	1	0	2
1	**0**	2	1	0
1	**1**	0	0	2
1	**1**	1	1	0
1	**1**	2	1	1
1	**2**	0	1	0
1	**2**	1	1	1
1	**2**	2	1	2
2	**0**	0	0	2
2	**0**	1	1	0
2	**0**	2	1	1

2	**1**	0	1	0
2	**1**	1	1	1
2	**1**	2	1	2
2	**2**	0	1	1
2	**2**	1	1	2
2	**2**	2	2	0



(a)

(b)



(c)

Figure 3.20**:** (a) Logic block diagram of the TFA as reported in [13] (b) Modified logic design of the TFA (c) The input output waveforms of the modified TFA

Literature reports design of ternary full adder by cascading two THAs [13]. As reported in [13], and illustrated in figure 3.20(a), the first THA adds two trits and the following THA adds the sum output from the previous THA with the C_{in} and generates 1-trit sum and 1-trit carry. The finally carry bit, C_{out} is generated by TOR gate operation between the two carry bits generated from the two stages (Half adder_1 and Half adder_2). The different waveforms for various input-output combinations are depicted in [13] which confirm the functionality of the reported approach.

A careful debugging of the circuit shown in figure 3.20(a), however, reveals a functionality issue in the design of full adder when A, B and$C_{in}$are all '2'. As per the reported block diagram, the final C_{out} is generated using TOR of the individual carry, produced by both the THAs. The ternary decoders used in the design of THA, deliver the output logic states '0' or logic state '2'.The truth table of the THA shows that the carry output will always have only any of the two logic states i.e either '0' or '1' for any combinations of input and the logic state '2' is never attained. It is therefore obligatory to use a TLS in the design of THA as indicated in figure. 3.20(a) and 3.20(b), so as to restrict the output to logic state '1'. The carry output, in such a design of TFA as reported in [13] will thus, be pulled on, at most to logic '1'. However, the input combination *A , B and*C_{in}*all '2'* demands the C_{out} to be at logic state '2'. The same fact is revealed by the equation for carry i.e. equation 3.11, which includes the term A^2, B^2 and C^2. It is impossible to obtain logic state '2' at the output of the TOR gate when the maximum logic state it receives at the input is '1'. The reported design of TFA does not consider the realization of the term $A^2B^2C^2$ of equation 12 and thus suffers from a functionality issue. It is thus necessary to modify the logic block diagram reported in [13] so as to

rectify the issue for the special case when C_{out} is required to be at logic state '2'. Figure 3.20(b) depicts the required modification in the design of TFA so as to confirm the functionality for all the combinations of the input. The simulation results of the modified circuit are shown in Figure 3.20(c). As expected, the individual carry of each THA (Half adder_1 and Half adder_2) is limited to logic '1' due to TLS. Because of the modified design, the final output C_{out} is at logic state'2' when A, B and C all are 2. The modified design requires only 36 ternary gates for the realization of TFA.

3.6.3 Ternary Multiplier [TM]

A Ternary Multiplier (TM) multiplies two ternary trit to generate a one trit product term and one trit carry term. The truth table for a one trit TM is shown in table 3.12. The logic equations derived from the K-map are detailed as in equation 3.12 and equation 3.13:

$$\text{Pr}\,oduct = (A^1B^2 + A^2B^1) + 1.(A^1B^1 + A^2B^2) \quad \text{.....3.12}$$

$$Carry = 1.(A^2B^2) \quad \text{.....3.13}$$

The equations 3.12 and 3.13 are implemented using the ternary decoder, TLS and the TAND and TOR gates. Similar to the THA, even in case of TM, further reduction in the number of circuit elements is achieved by replacing the ternary logic gates in the highlighted block by binary logic gates. The MIFGMOS transistor based binary AND and binary OR logic gates as indicated in Figure. 3.21(a) are used in the TM. The input-output waveform of the designed TM is shown in figure 3.21(b). As expected, the presented approach achieves further reduction in the circuit element count. The designed MIFGMOS TM is further analyzed in terms of the transient response and compared with the state of art methods.

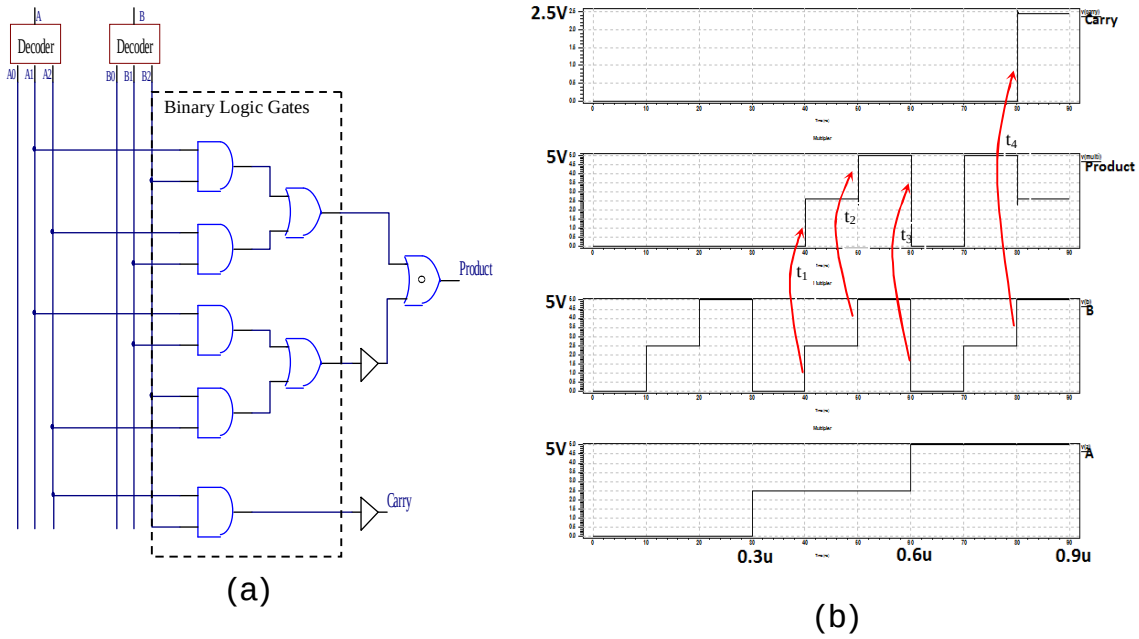


Figure 3.21: (a) MIFGMOS transistor based ternary multiplier using binary gates (b) The input-output waveforms of the ternary multiplier

Table 3.12: Truth table of Ternary Multiplier

Input		**Multiplier**	
A	**B**	Product	Carry
0	**0**	0	0
0	**1**	0	0
0	**2**	0	0
1	**0**	0	0
1	**1**	1	0
1	**2**	2	0
2	**0**	0	0
2	**1**	2	0
2	**2**	1	1

3.6.4 Ternary Half Subtractor (THS)

The Ternary Half Subtractor (THS) accepts two 1-trit ternary numbers and produces 1-trit difference between the two ternary inputs. 1-trit borrow is also generated as one of the outputs. The truth

table of the THS is represented in table 3.13. The logic functions given by equation 3.14 and equation 3.15 obtained from the Karnaugh Map are used to realize the ternary half subtractor. The functional logic diagram of the MIFGMOS based transistor of THS is illustrated in figure 3.22(a) and figure 3.22(b) illustrates the input output waveform. The designed MIFGMOS THS is further analyzed in terms of the transient response and compared with the state of art methods.

$$Difference = (A^0B^1 + A^1B^2 + A^2B^0) + 1.(A^0B^1 + A^0B^2 + A^1B^2) \quad \ldots 3.14$$

$$Borrow = 1.(A^0B^1 + A^0B^2 + A^1B^2) \quad \ldots 3.15$$

Table 3.13: Truth table of THS

Input		**THS**	
A	**B**	Difference	Borrow
0	**0**	0	0
0	**1**	2	1
0	**2**	1	1
1	**0**	1	0
1	**1**	0	0
1	**2**	2	1
2	**0**	2	0
2	**1**	1	0
2	**2**	0	0

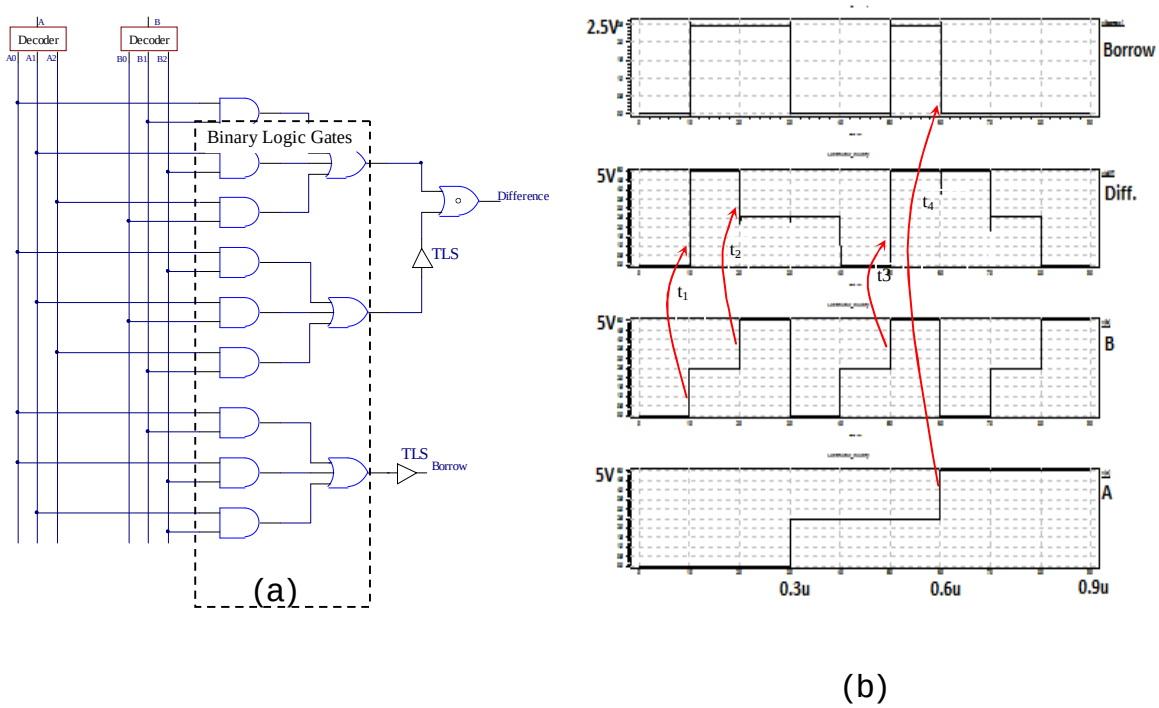


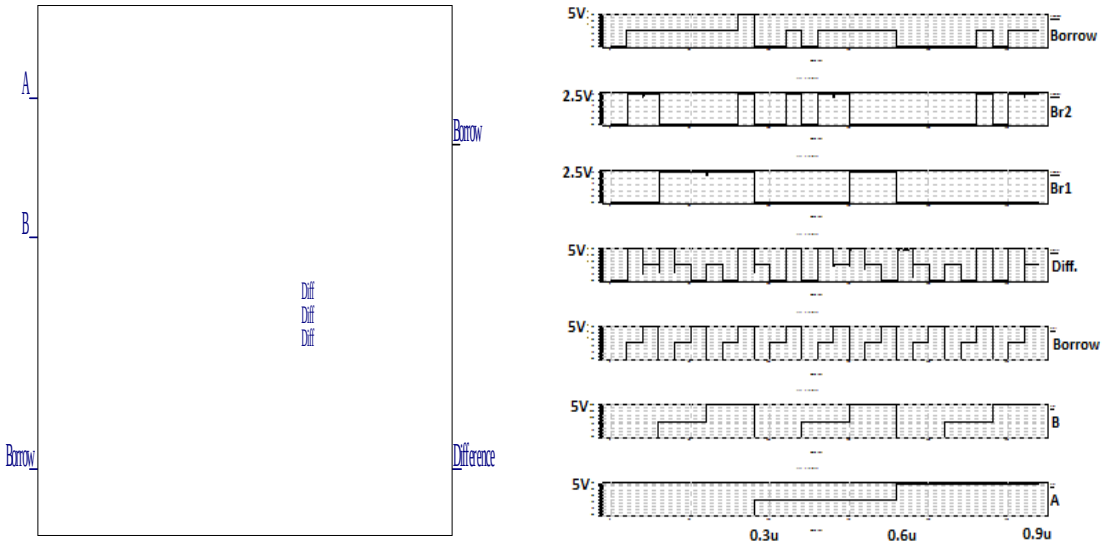
Figure 3.22: (a) MIFGMOS transistor based THS using binary gates (b) The input-output waveforms of the THS

3.6.5 Ternary Full Subtractor (TFS)

A 1-trit Ternary Full Subtractor (TFS) subtracts three 1-trit numbers to produce two outputs, difference and borrow. As shown in figure 3.23(a) TFS is designed using a cascade combination of two THS. Similar to TFA, when the ternary inputs, *A,B and Borrow all are '2'* the expected outputs, difference and borrow both are at logic state '2'. This condition has been taken care of by using an additional TAND gate at the final stage as indicated in the logic block diagram figure. 3.23(a). The input output waveforms are shown in figure 3.23(b).

Table 3.14: Truth table of Ternary Full Subtractor

Inputs			**TFS**	
A	**B**	C_{in}/Borrow	Borrow	Difference
0	**0**	0	0	0
0	**0**	1	1	2
0	**0**	2	1	1
0	**1**	0	1	2
0	**1**	1	1	1
0	**1**	2	1	0
0	**2**	0	1	1
0	**2**	1	1	0
0	**2**	2	2	2
1	**0**	0	0	1
1	**0**	1	0	0
1	**0**	2	1	2
1	**1**	0	0	0
1	**1**	1	1	2
1	**1**	2	1	1
1	**2**	0	1	2
1	**2**	1	1	1
1	**2**	2	1	0
2	**0**	0	0	2
2	**0**	1	0	1
2	**0**	2	0	0
2	**1**	0	0	1
2	**1**	1	0	0
2	**1**	2	1	2
2	**2**	0	0	0
2	**2**	1	1	2
2	**2**	2	1	1



(a) (b)

Figure 3.23: (a) Modified logic design of TFS (b) Input output waveforms of the TFS

3.6.6 Ternary Comparator (TC)

A 1-trit Ternary Comparator (TC) compares two ternary trits, A and B to produce one of the three outputs, $A > B$, $A < B$ and $A = B$ based on the relation between the two input signals. The corresponding output is either at logic '0' or '2'. The truth table of the TC is shown in table 3.15. The logic equations for the realization of the ternary comparator are given by equation 3.16, 3.17 and 3.18 and used to realize TC using MIFGMOS transistor based binary AND and OR gates as indicated in Figure. 3.24(a).

$$A < B = (A^0B^1 + A^0B^2 + A^1B^2) \quad \text{.....3.16}$$

$$A = B = (A^0B^0 + A^1B^1 + A^2B^2) \quad \text{.....3.17}$$

$$A > B = (A^1B^0 + A^2B^0 + A^2B^1) \quad \text{.....3.18}$$

The input-output waveform of the ternary comparator is illustrated in figure 3.24(b). The designed MIFGMOS TC is further analyzed in terms of the transient response and compared with the state of art methods.

Table 3.15: Truth table of Ternary comparator

Input		**Comparator**		
A	**B**	A=B	A<B	A>B
0	**0**	2	0	0
0	**1**	0	2	0
0	**2**	0	2	0
1	**0**	0	0	2
1	**1**	2	0	0
1	**2**	0	2	0
2	**0**	0	0	2
2	**1**	0	0	2
2	**2**	2	0	0

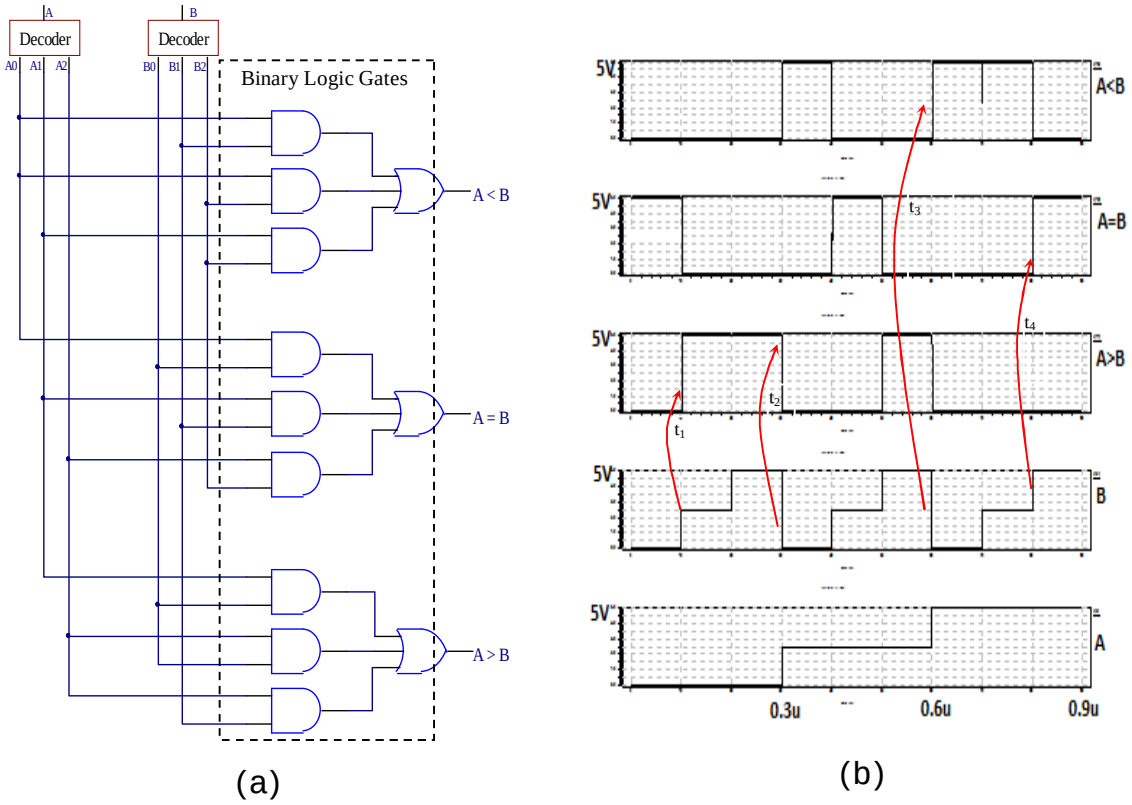
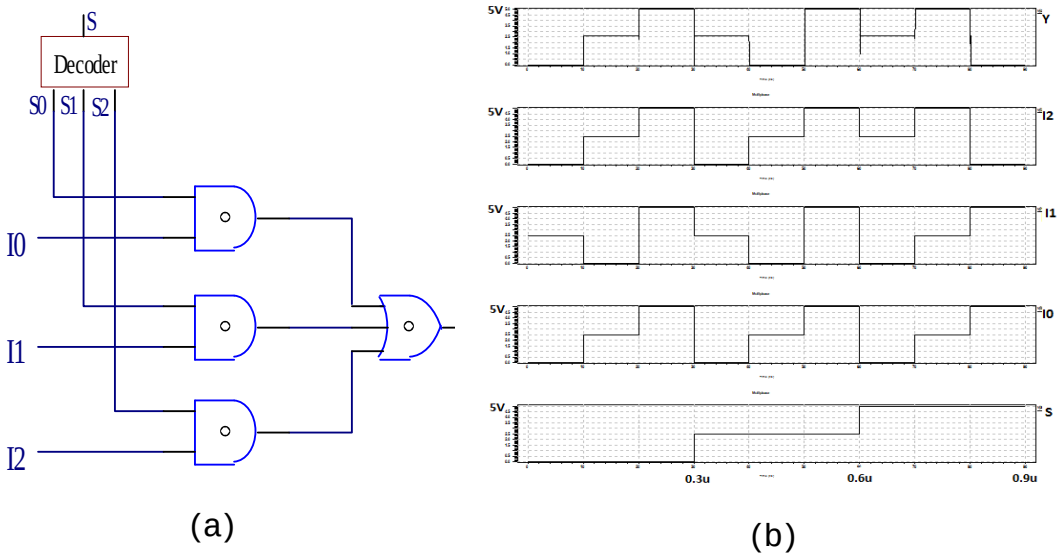


Figure 3.24: (a) MIFGMOS transistor based TC using binary gates (b) The input-output waveforms of the TC

3.6.7 Three-to-one Ternary Multiplexer

Similar to a binary multiplexer, a 3:1 ternary multiplexer selects one of the inputs I_0, I_1 and I_2 based on the combination of the select line. The select line S is decoded by the ternary decoder to produce three outputs, S_0,S_1 and S_2. The select lines decide the input that appears at the output Y. Figure 3.25(a) illustrates the logic diagram of the ternary multiplexer and the input output waveforms are depicted in figure 3.25(b).



(a) (b)

Figure 3.25: (a) MIFGMOS transistor based ternary multiplexer using binary gates (b) The input-output waveforms of the ternary multiplexer.

3.6.8 Discussion on MIFG based TALU

This research presents an efficient hybrid approach based on combination of Multi Input Floating Gate Metal Oxide Semiconductor(MIFGMOS) transistor and conventional MOSFET for the realization of the Ternary Arithmetic and Logic Unit (TALU).

The MIFGMOS based designed TALU demonstrates expected functionality and additionally signify good improvement in the performance parameters. The advantages of the devised hybrid

MIFGMOS transistor based TALU are apparent from the significant reduction of the circuit elements when compared with the CNTFET [1] and QDGFET [13] based approaches reported in the literature.

The hybrid approach presented in this research combines the virtues of both the devices and specifically takes advantage of tunability and controllability of MIFGMOS transistor to facilitate the significant reduction in the circuit element count of the ternary combinational circuits as compared to earlier reported methods. It must be emphasized that use of MIFGMOS based binary gates in the ternary combinational circuits has achieved further reduction in the circuit element count, ensuring the improvement in the timing analysis.

The simulation results of the transient timing exhibit an improvement in the performance parameters. The reduction in the number of the gates due to use of MIFGMOS transistor obviously lead to improvement in the delay.

3.7 MIFG Based Design of Ternary Sequential Circuits

Combinational and sequential circuits, both play a significant role in any processor or a digital system. The designed ternary gates are further extended to realize ternary flip-flap-flop and counter from the perspective of a ternary processor.

3.7.1 D Latch

A simple ternary D latch is designed akin to the binary D latch. However, ternary D Latch will obviously deliver three logic levels, 0, 1 and 2 and are therefore popularly called as flip-flap-flop in contrast to a binary flip-flop that delivers only 2 states. Ternary NAND gates are

cross coupled to deliver complementary outputs $Q$and $\bar{Q}$. Under normal conditions these outputs will always be inverse of each other.

The designed D flip-flap-flop will respond to the positive edge trigger at the binary clock input at the various inputs. Its functionality is detailed in the table 3.16 and the logic diagram and obtained waveforms are depicted in figure 3.26 and figure 3.27 respectively.

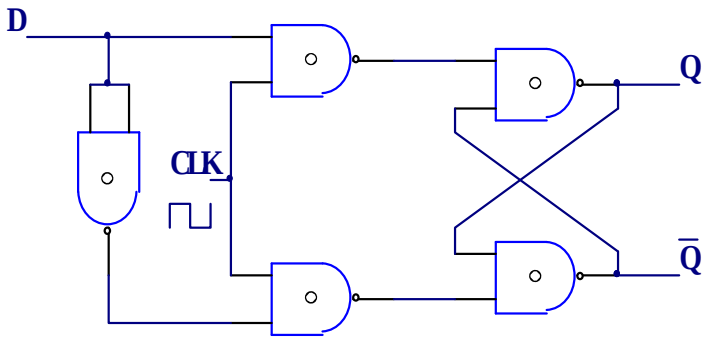


Figure 3.26: D flip-flap-flop

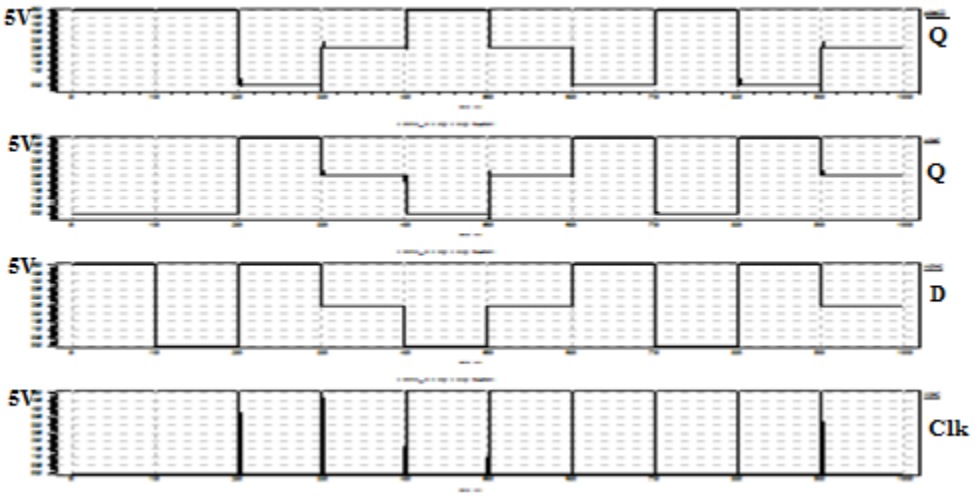


Figure 3.27: Input and output waveform of D flip-flap-flop

Table 3.16:Truth table of D flip-flap-flop

CLK	D	Previous state		Next State	
		Q	$\bar{Q}$	Q	$\bar{Q}$
↟	0	2	0	0	2
↟	1	2	0	1	1
↟	2	2	0	2	0
↟	0	1	1	0	2
↟	1	1	1	1	1
↟	2	1	1	2	0
↟	0	0	2	0	2
↟	1	0	2	1	1
↟	2	0	2	2	0
0	X	Latch		Previous state	

Table 3.17: Dynamic Characteristics of D flip-flap-flop

Pd	$Clk - Q$	23pS
Pd	$Clk - \bar{Q}$	37pS
t_r	t_r	24pS
t_f	t_f	42pS

3.7.2 Ternary Counter

A two trit synchronous ternary counter is further designed using the D latch gate to obtain 3^2 states as shown in figure 3.31. These 9 states are tabulated in table 3.20. Usually in a binary synchronous counter, a dedicated combinational circuit that serves as an input to generate the desired next state is required only in 3 bit counter. However in a ternary counter such a combination is of paramount necessity even in a 2-trit counter. This research presents a ternary counter, using

already designed D flip-flop and additionally needs the following circuits for its operation:

- Binary Clock: Unavailability of the traditional crystal to generate a ternary clock makes it mandatory to use existing binary clock itself for any ternary sequential circuit
- A combinational circuit: To generate ternary voltage levels 0,1 and 2 at the input of the D flip-flop so as to finally achieve the same voltage levels at the output in terms of the various states.

This research presents a novel approach to obtain the ternary voltage levels from the binary clock. As represented in the truth table 3.18 and section 3.6.1 of this chapter, it is evident that when one of the input is at logic 'n' and having the other input connected permanently at logic state '1' , delivers the n+1 state at the output. This ultimately produces ternary logic state '1' , '2' and '0' at the output when the input is at state '0', '1' and '2' respectively as highlighted in the table 3.18. Figure 3.28 depicts the circuit delivering the required ternary sequence. It thus functions as a one-trit counter and also as a ternary clock.

Table 3.18: Truth table of Half adder

A	B	Sum
0	0	0
0	1	1
0	2	2
1	0	1
1	1	2
1	2	0
2	0	2
2	1	0
2	2	1

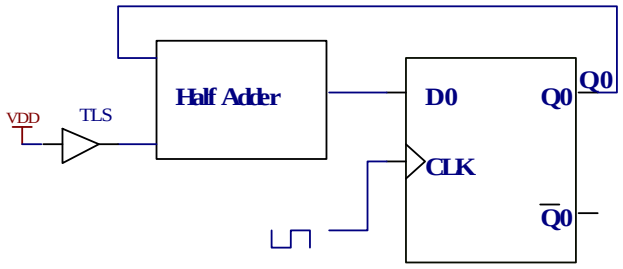


Figure 3.28: 1 trit counter

Input to D0= $(A^0B^2 + A^1B^1 + A^2B^0) + 1.(A^0B^1 + A^1B^0 + A^2B^2)$ ...3.19

Modified Ternary Counter:

As already explained, it is only logic '1' which plays a crucial role in the generation of the ternary states. Thus only three rows of the table 3.19 are required to be actually considered, when designing the combinational circuit for the ternary counter. Table 3.20 represents the required combination of the inputs

The logic equation can be easily derived for its realization at the input of the D Flip flop. Comparing the equation 3.19 and 3.20,it is apparent that the number of circuit elements gets reduced. A ternary half adder requires 11 gates and 2 decoders, which is very effectively reduced to 3 gates and 1 decoder. The modified circuit diagram is illustrated in figure3.29.

Table 3.19: Required truth table for counter

Q	A	Input (I)
0	1	1
1	1	2
2	1	0

$$I = Q^1A^1 + 1.(Q^0A^1) \quad .....3.20$$

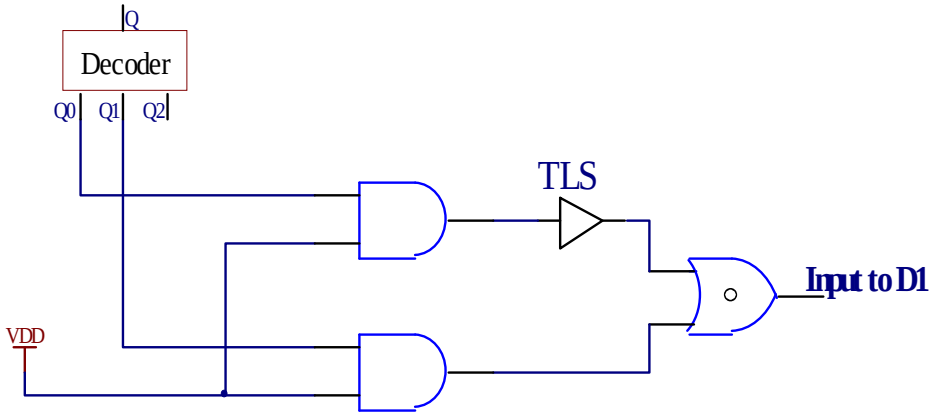


Figure 3.29: Modified combinational circuit for 1 trit counter

Table 3.20: Required truth table for 2nd stage of counter

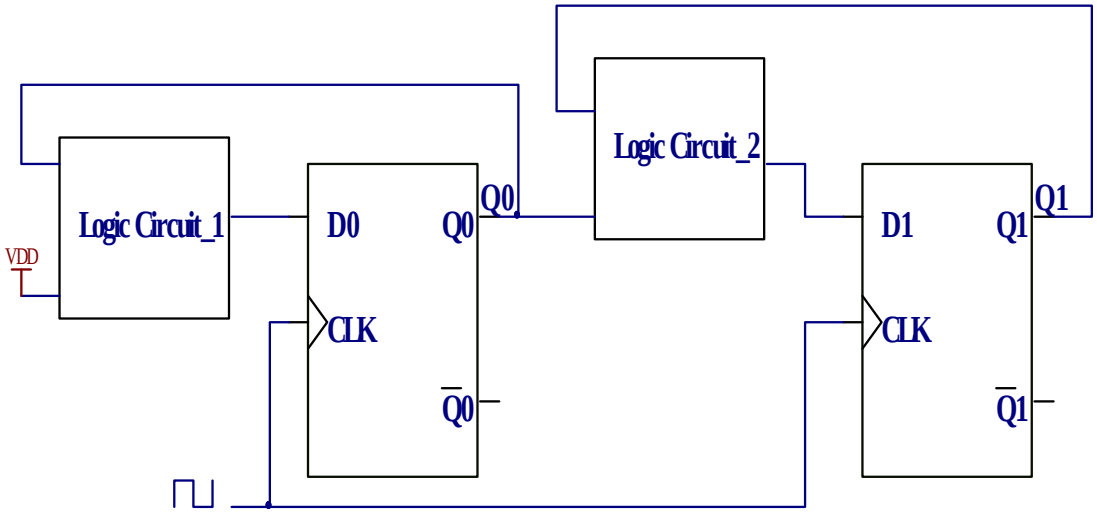
CLK	(Q_1)	(Q_0)	Input (D_1)
↑	0	0	0
↑	0	1	0
↑	0	2	1
↑	1	0	1
↑	1	1	1
↑	1	2	2
↑	2	0	2
↑	2	1	2
↑	2	2	0

$$D_1 = (Q_1^1 Q_0^2 + Q_1^2 Q_0^0 + Q_1^2 Q_0^1) + 1.(Q_1^0 Q_0^2 + Q_1^1 Q_0^0 + Q_1^1 Q_0^1) \quad \text{.....3.21}$$

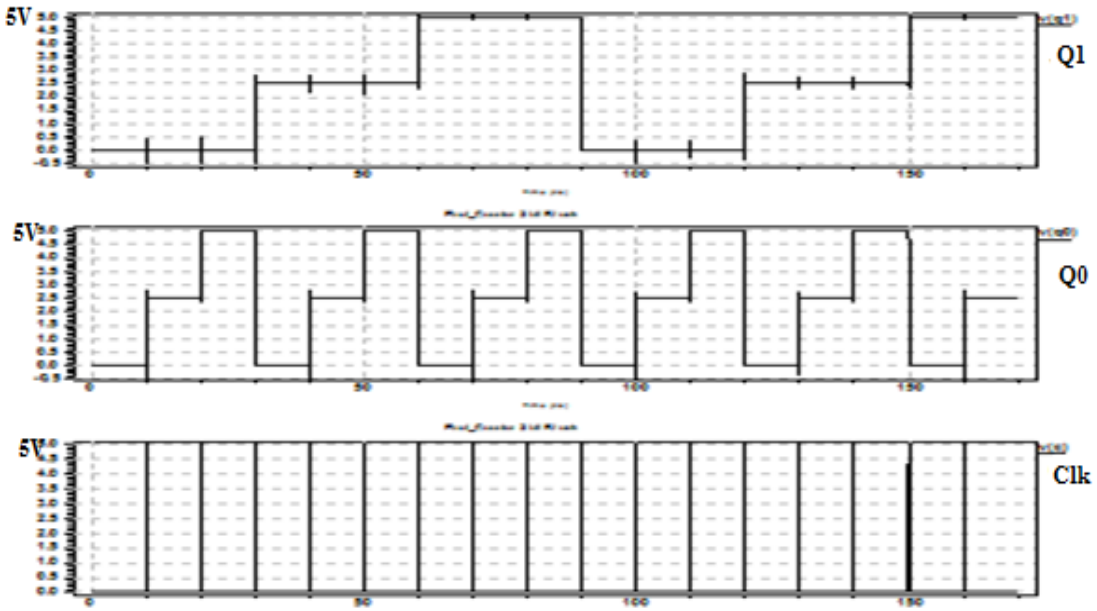
The same circuit illustrated in figure 3.29 can further be extended to function as a two-trit counter as represented in figure 3.30. Logic Circuit_1 and Logic circuit_2 in figure 3.30 represent the combinational circuits which is required in design of the synchronous counters.Logic circuit_1 represents the circuit illustrated in figure

3.30.Logic circuit_2 for the 2nd stage of the counter is derived using the functionality detailed in the table 3.20.

Equation 3.21 represents Logic_circuit_2, which acts as an input for the next stage, i.e. D1.



(a)



(b)

Figure 3.30: (a) 2 trit counter (b) Input and Output waveform of 2nd trit counter

3.7.3 Discussion on MIFG based ternary sequential circuits

Ternary sequential circuit, a D Flip-Flap-Flop is designed and its functionality is verified. Further, a ternary counter is realized which uses the D flip-flap-flop and the existing binary clock. An intelligently designed combinational circuit for the generation of the ternary states in a ternary counter ensures the reduction in the circuit element count.

3.8 In a Nutshell

With the recent technological advancements, commercial realization of ternary circuits is being watched with keen interests. This research presents an efficient hybrid approach based on combination of MIFGMOS transistor and conventional MOSFET for the realization of the Ternary combinational and sequential circuits.

The MIFMOS transistor based binary gates and hybrid MIFGMOS transistor based ternary gates are initially designed and effectively simulated. MIFGMOS transistor based binary NOR gate is used to modify the design of ternary decoder that leads to reduction in circuit element count.

A novel TLS that has received meager attention in the reported literature is also presented in this research. It exploits the controllability and tunability of the MIFGMOS transistor to achieve an intermediate voltage level and thereby the desired functionality of the level shifter. Moreover, the need of passive components and an additional power supply is completely eliminated leading to considerable reduction in the power.

This research further identifies a functionality issue in the reported design of TFA and presents a solution to the identified problem. TFS using two THS and various other ternary combinational circuits are designed and simulated using the designed ternary and

binary gates, modified ternary decoder and novel TLS.

An extensive simulation of the designed TALU is carried out for nine operations using TSPICE circuit simulator. The designed hybrid TALU demonstrates expected functionality and additionally signify good improvement in the performance parameters. The advantages of the novel hybrid MIFGMOS transistor based approach for the TALU are apparent in terms of the circuit element count as compared to the earlier reported methods. It must be emphasized that use of MIFGMOS based binary gates in the ternary combinational circuits has achieved further reduction in the circuit element count, ensuring the improvement in the timing analysis.

The simulation results of the transient timing exhibit an improvement in the performance parameters. The reduction in the number of the gates due to use of MIFGMOS transistor obviously lead to reduction in the delay. The transient response of the designed ternary combinational circuits demonstrate its functionality for various loads and at various operating frequencies ranging from 500 KHz to 5 MHz. Acceptable voltage levels were obtained at the output for all these variations. This signifies good fan-out values of the designed ternary gates, which is an apparent advantage of operating MIFGMOS transistors at 5V. Another apparent advantage of using 5V as the operating voltage is the higher noise margins which are of paramount importance from the prospects of ternary processor.

Another important point to be noted is the use of resistors in the designed ternary circuits. As the model parameters for MIFGMOS transistor are not available, hence standard MOS models are used to simulate these structures. The electrical components are added to the standard MOS models to emulate the MIFGMOS transistor behavior. The equivalent circuit of MIFGMOS transistor contains various

capacitors. When this circuit is simulated using TSPICE, the problem of floating nodes arises, as a result the simulations fail to converge. As TSPICE cannot accept floating nodes having no dc path to ground, resistors are used to bypass each capacitor with a resistor. The role of these resistors is restricted only to simulation and is not considered in the layout of the circuits. The on-chip area is therefore not compromised.

Ternary sequential circuit, a D Flip-Flap-Flop is further designed and its functionality is verified. The design is extended to realize a ternary counter which uses the existing binary clock and an intelligently designed combinational circuit for the generation of the ternary states.

The simulation results and the transient analysis of the devised ternary combinational circuits and the sequential circuits confirm the authenticity of the novel hybrid MIFGMOS transistor based approach as well as the superiority of the devised ternary circuits specifically in terms of the circuit element count and performance parameters in comparison with the other state-of-the-art ternary circuits.

CHAPTER 4
TESTING AND SIMULATION OF THE EXTENDED TERNARY LOGIC MODULES

The CMOS and MIFG based implementation represent device level approach to implement various ternary circuits. It is necessary to further extend this approach to incorporate additional inputs and functionality in the designed ternary combinational and the sequential circuits from the perspective of the ternary processor. Arithmetic logic unit and a control unit are the fundamental building block of any processor. The task of effectively designing the TALU and control unit for a ternary processor has received comparatively less attention by the researchers and to the best of our knowledge, meager work is reported in the literature addressing this concern. This research addresses this concern and thus extends the MIFG based ternary circuits designed earlier to design and simulate TALU and a control unit. This chapter details the use of Very-High-Speed Integrated Circuits, VHSIC, Hardware Description Language (VHDL) formulated in this research for the design and implementation of:

- Vectored ternary ALU (4-trit) using the sub-program overloading
- An efficient Ternary Control Unit (TCU) for a ternary processor

4.1 Ternary ALU

This research presents an efficient technology dependent method for defining, analyzing, testing and implementing the ternary ALU using VHDL. The designed 4 – trit Ternary ALU (TALU) performs

ternary addition, subtraction and logical TNOT, TAND and TOR operations.

4.1.1 Research Methodology for Designing TALU

The block diagram of the designed TALU is depicted in Figure 4.1. The designed TALU has two 4-trit inputs 'A' and 'B', 3-trit select lines, 'S_2', 'S_1','S_0' and outputs 'Y' and 'Carry/ Borrow'. For the sake of simplicity the inputs and the outputs in the block diagram of 4-trit TALU are depicted as 1- trit, however they are in actual, simulated as 4-trit. TALU has arithmetic and a logical unit which is selected by the ternary multiplexer. Three select lines of the multiplexer enables it to select amongst 27 inputs (3^3 = 27). Figure 4.1 details the block schematic of the designed TALU and the operations are detailed in table 4.1. The devised research approach is restricted to only 18 operations, which can be easily enhanced further by declaring additional ternary packages.

The research methodology for designing ALU can be envisioned in the following two parts:

- Developing VHDL constructs to support Ternary number system
  a. Ternary data types
  b. Package declaration
  c. Functions for ternary logic operation and ternary arithmetic operation
- Design and verification of operational functionality of TALU using a bottom - up approach.

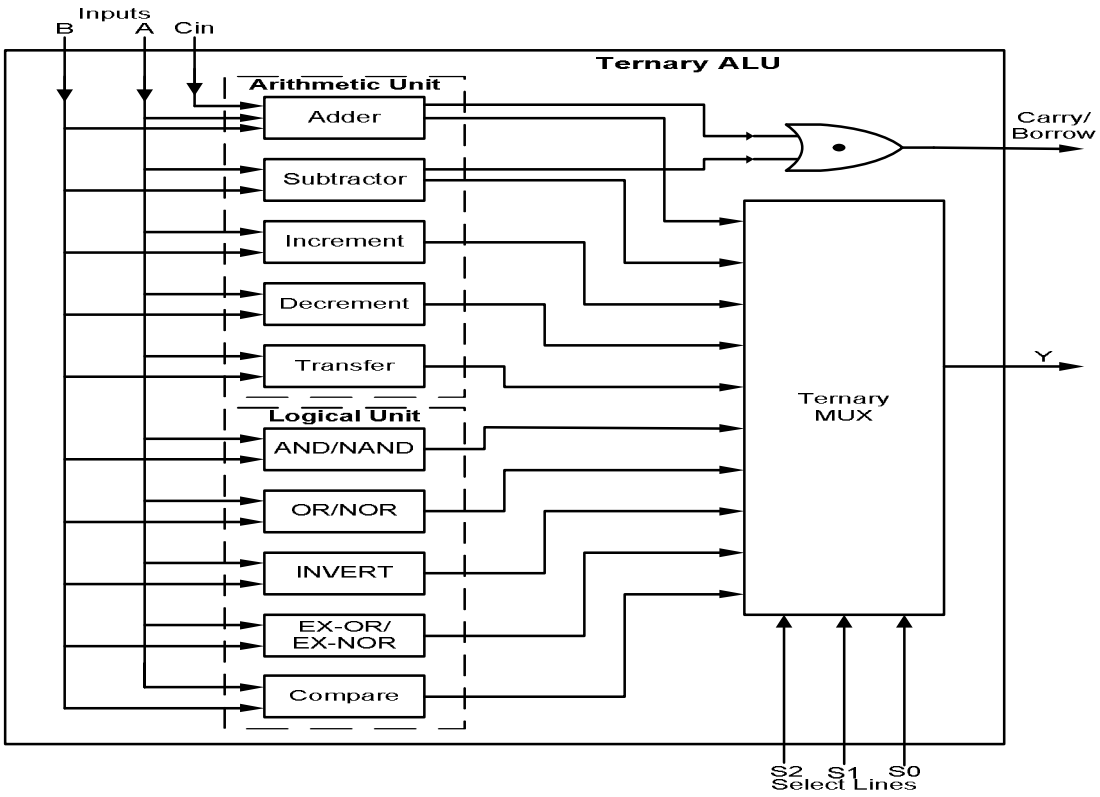


Figure 4.1 Block schematic of the TALU

Table 4.1: Select line combinations for various arithmetic and logical operations

Select Line			Arithmetic Operations
S_2	S_1	S_0	
0	0	0	Add A and B
0	0	1	Add A and B with carry
0	0	2	Subtract B from A
0	1	0	Transfer A
0	1	1	Increment A
0	1	2	Decrement A
0	2	0	Transfer B
0	2	1	Increment B
0	2	2	Decrement B

Select Line			Logical Operations
S_2	S_1	S_0	
1	0	0	Invert A
1	0	1	Invert B
1	0	2	AND A with B
1	1	0	OR A with B
1	1	1	NAND A with B
1	1	2	NOR A with B
1	2	0	XOR A with B
1	2	1	XNOR A with B
1	2	2	Compare A with B

(i) Developing VHDL Constructs To Support Ternary Number System:

VHDL is reported to be popularly used hardware description language for modeling of numerous digital systems. VHDL is technology independent language, and is therefore portable and reusable. It provides the capability for creating user-defined types that can be used to model and simulate the desired system. The designed TALU uses three logic levels: logic '0', '1' and '2'. It is therefore necessary to develop specific ternary data types, package declaration and functions for the designed TALU.

(a)Ternary Data Types:

VHDL supports MVL by means of standard package std_logic_1164. This package includes 9 logic levels i.e. *U: uninitialized, X: unknown , 0: Logic 0 , '1: Logic 1 , Z : high impedance , W : weak unknown , L : weak zero, H: weak 1, - : don't care.* The package declaration is predominantly from the perspective of binary logic. They are built on Boolean algebra and are applied to the modeling of 2-valued logic circuits. In the context of ternary logic, wherein the radix of operation is 3, a user defined data type ***'TERNARY_LOGIC'*** is declared to support three values: '0', '1', '2'. An unconstrained array data type ***'TERNARY_LOGIC_VECTOR'*** is additionally declared to support ternary vector inputs and outputs. The VHDL construct for data type declaration is as follows:

```
-- Un-resolved Ternary logic state
    TYPE ternary_ulogic IS ('0','1','2',);
```

(b) Package Declaration

The package provides a convenient mechanism to store and share declarations that are common across many design units. A package is represented by package declaration and optionally a package body. To support ternary number system with 3- valued logic there is a need to develop a separate package. Therefore ***'TERNARY_TYPES'*** package is developed. 'TERNARY_TYPES' package contains a set of declaration like data types and function required for implementation of ternary system. The construct below details the package declaration, function declaration and data types.

```
PACKAGE ternary_types IS
        -- Resolved Ternary Logic states

SUBTYPE ternary_logic IS resolved ternary_ulogic;
        -- Unconstrained array of ternary_logic
        -- for use in    declaring signal arrays

TYPE ternary_logic_vector IS ARRAY (NATURAL RANGE<>) OF ternary_logic;
        -- Function Declaration without operator overloading

FUNCTION stnot (l: ternary_logic) RETURN ternary_logic;
        --  Function Declaration with operator overloading

FUNCTION "not" (l: ternary_logic) RETURN ternary_logic;
END ternary_types;
```

The main data type '*ternary_ulogic*' is unresolved initially. The declared subtype '*ternary_logic'* is associated with resolution function. A resolution function is used to return the value of a signal when the signal is driven by multiple drivers [51]. Function '*stnot'* is declared for ternary inverter as indicated. Similarly, other logical and arithmetic operations are also declared using function.

(c) Functions for Ternary Logic Operation and Arithmetic Operation

To perform the basic ternary logic and arithmetic operations, operation specific declaration of the corresponding ternary function is required. The different operations supported by TALU are detailed in table I. The truth tables for the Ternary logic gates (TNOT, TAND, TOR, TNAND, TNOR, TXOR, TXNOR) are used to declare the functions for the respective operations. The declared functions accommodated vectored inputs. Operators for the logical operations *(and, not, or, nor, xor, xnor)* were overloaded for enhancing the flexibility and the reusability of the design. Subprogram overloading allows the designer to write multiple subprograms with the same name but the number of arguments, type of arguments and return values can be different. The VHDL compiler during the compile time selects the subprograms that match the subprogram call. If no subprogram matches the call, an error is generated. Overloaded functions are defined for scalar and vector data types. Ternary arithmetic operations were handled using ternary logic gates.

```
PACKAGE BODY ternary_data_types IS
--Truth Table for S_Ternary NOT function
 CONSTANT stnot_table : t_logic_ld := ('2','1','0');
-- Function for Ternary NOT Gate with overloading
FUNCTION "NOT" (l: ternary_logic)
RETURN ternary_logic IS
BEGIN
      return (stnot_table(l));
END "NOT";
```

```
-- Function for Ternary NOT Gate without overloading
FUNCTION STNOT (I: ternary_logic)
RETURN ternary_logic IS
BEGIN
        return (stnot_table(I));
END STNOT;
END ternary_data_types;
```

The function body of the declared function is described in the package body. The operator overloading for '*NOT'* is used. It must be noted that both the functions '*NOT*' and '*STNOT*' are functionally similar, however the profile of the functions (parameters passed to it) differs as indicated below.

```
--Use of function without operator overloading
Y <= STNOT (A);
-- Use of function with operator overloading
Y <=  NOT A;
```

Figure 4.2 illustrates the concept of sub-program overloading used in the VHDL implementation of the designed TALU. Standard Package has the definitions of the binary gates, whereas the user defined, Ternary Package comprises of the functionalities of Ternary gates. Figure 4.2 shows an example of NOT gate. The parameters passed in the profile select the appropriate package and definition to deliver to expected output.

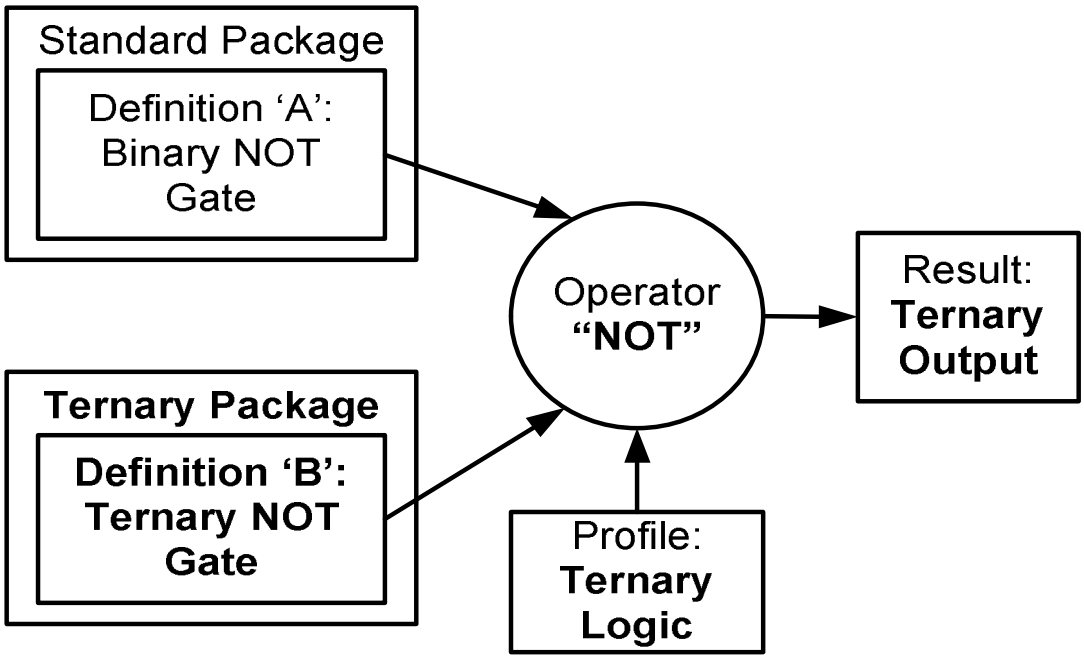


Figure 4.2: Concept of sub-program overloading

(ii) Design and VHDL Implementation

As mentioned in system design, various operations can be performed using the ternary ALU. The VHDL code and test bench is written to verify the functionality of each and every 4-trit operation supported by Ternary ALU using the developed VHDL constructs. Figure 4.3 describes the test bench created for the functional and the gate level simulation of theTALU. A bottom up approach is used to verify the operational functionality of the designed TALU. Random number generator generates various combinations of the input A and B for the arithmetic or the logical operation as specified using the select lines.The designed TALU is considered as the Device Under Test (DUT). The combinations on the select lines are generated using a sequence generator. Sub–program overloading has been effectively used to design ternary logical and arithmetic operators. VHDL supports multi valued logic and is therefore preferred to exploit its usefulness in sub–program overloading.

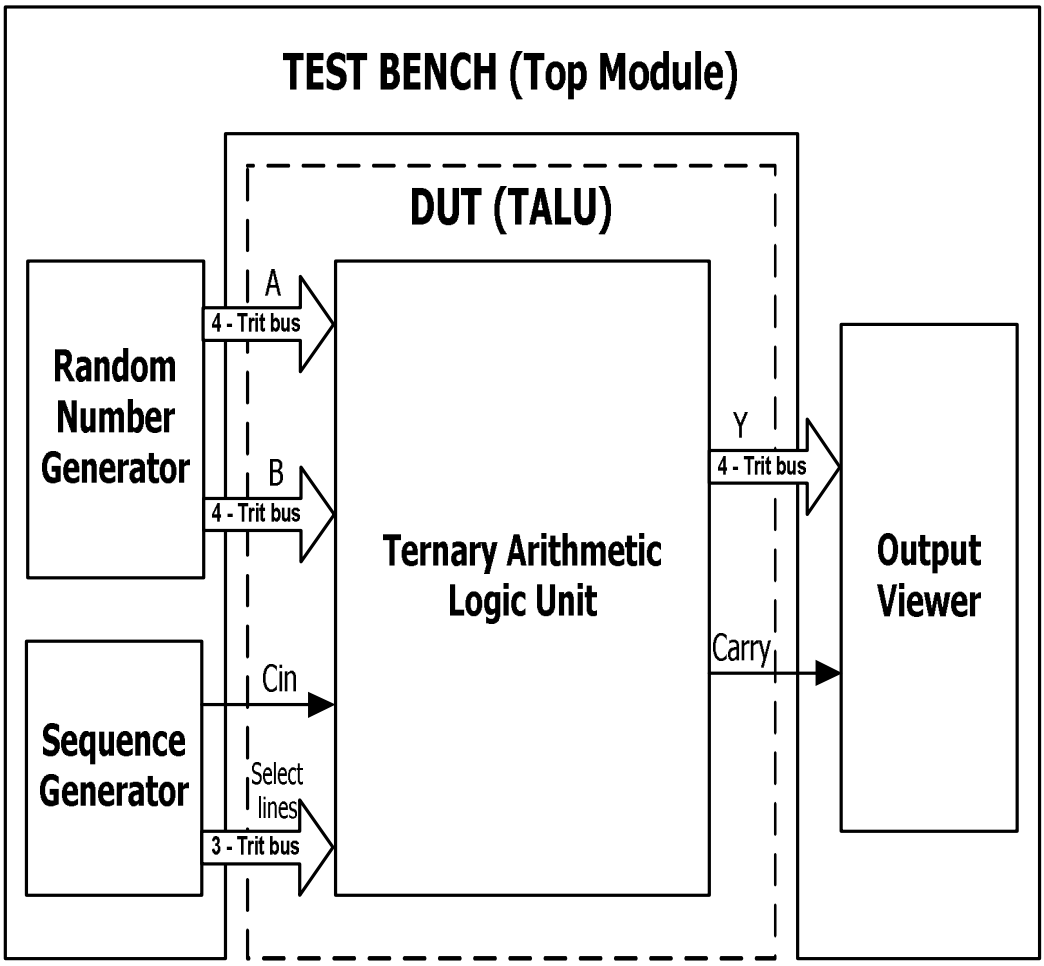


Figure 4.3: Testing and verification of the TALU

4.1.2 Simulation Results

The devised TALU is implemented using VHDL, Xilinx 14.2 ISE version and ModelSim 6.5. Figure 4.4 illustrates the simulation results of ternary arithmetic unit. As depicted the arithmetic operations addition, addition with carry, subtraction, transfer, Increment.

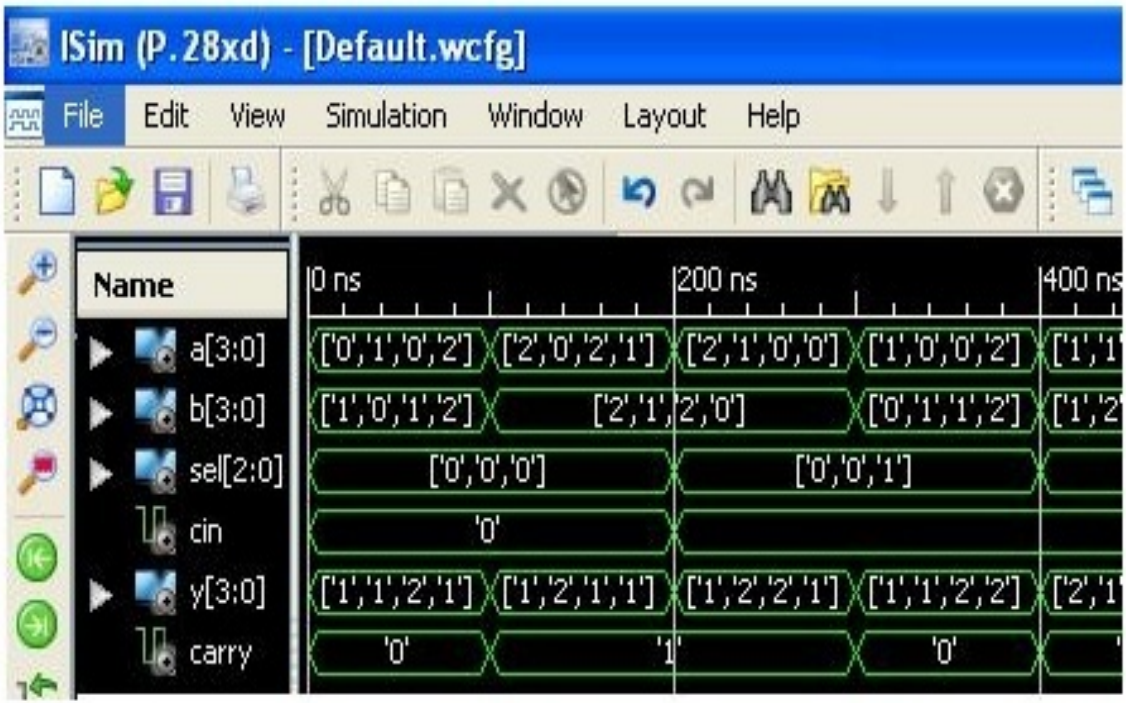


Figure 4.4: Simulation results of various arithmetic operations without considering the delay component.

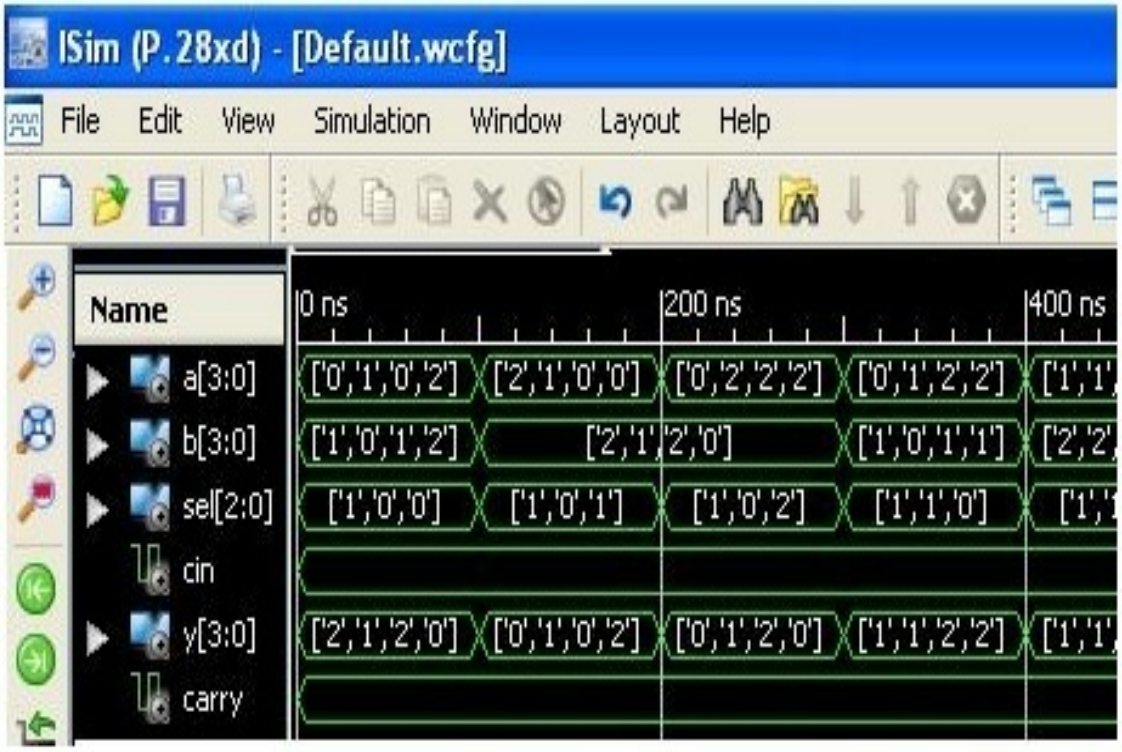


Figure 4.5: Simulation results of various logical operations without considering the delay component

Signals Y and carry signify the appropriate and expected results as driven by the input signal and the select lines. Figure 4.5 similarly shows the simulation results of corresponding logical operations. It must however be noted that the carry signal play a relevant role only in arithmetic operations. As expected from the perspective of any processor, the carry signal remains at a low level during the logical operations. It must also be noted that the simulation results in figure 4.4. and figure 4.5 signify only functional simulation of the TALU. A practical realization of TALU will face many important considerations and performance issues. Not all of these issues can be addressed and predicted when working in simulation environment. However, VHDL supports various levels of abstraction for improved performance analysis of the system. The performance analysis of the TALU is examined using gate level modeling. Propagation delay is incorporated in the presented design to perform the timing analysis. Figure 4.6 and figure 4.7 depict the gate level simulation of arithmetic and logical operations considering the propagation delay in practical circuits. In the simulation of the design with delay considerations a delay of ’10 ns ’ has been chosen with reference to the earlier reported research. As manually highlighted in figure 4.6, (with delay); a delay of 60 ns in the output signal ‘Y’ has been observed for the arithmetic operations. A similar delay has also been observed in logical operations. However, in logical operations the delay is relatively less. The arithmetic circuits require more hardware [number of gates for respective circuit realization] as compared to the logical circuits. The increased delay in arithmetic operations is therefore well justified and supported by the literature. Operation of “Add with carry” requires more time as compared to other operation. It is therefore critically analyzed and highlighted (with a red arrow) in Figure 4.6. As depicted, select line

combination 001 indicates add with carry operation and the results are delayed.

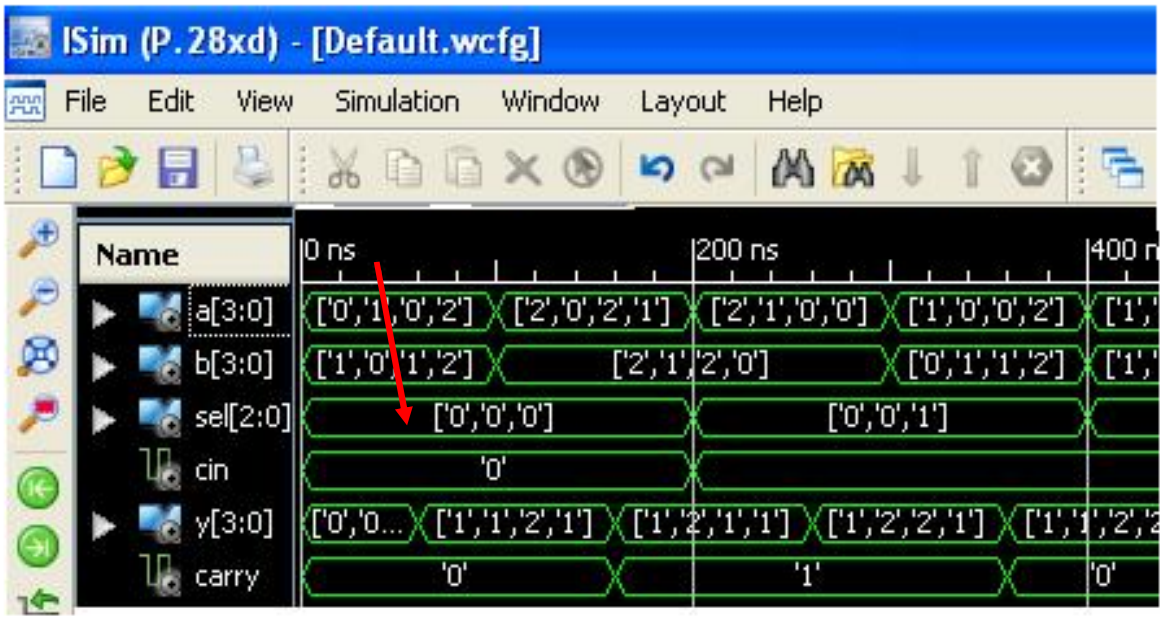


Figure 4.6: Simulation results of various arithmetic operations with considering the delay component

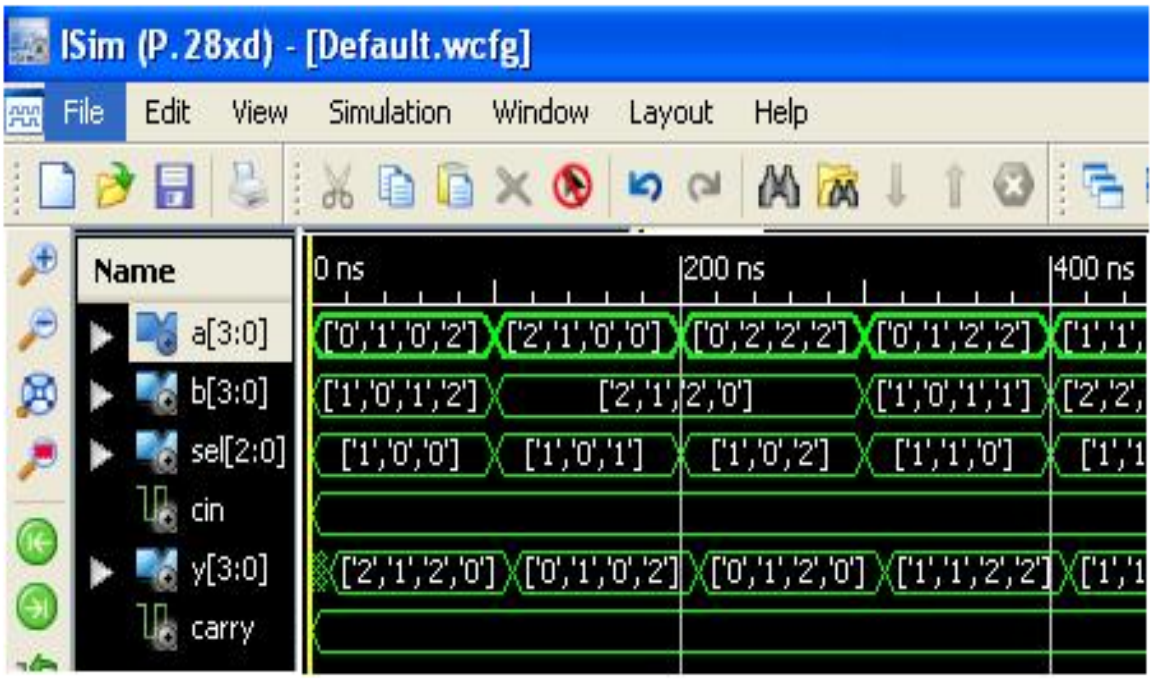


Figure 4.7: Simulation results of various logical operations considering the delay component

4.1.3 Discussion

An efficient method for defining, analyzing, testing and implementing vectored ternary ALU is developed in this research. Altogether 18 operations are implemented in the TALU developed from the perspective of ternary processor. A detailed technology dependent timing analysis of the designed TALU has been carried out using VHDL. The implementation of sub program overloading feature in the presented TALU makes its design unique, flexible and portable for further extension. Such designs are preferred and imperative in rapid and explosive advancements in digital environment. The designed 4 – trit ternary ALU performs substantial arithmetic and logical operations from the perspective of multi valued systems. The timing performance of the devised ALU signifies encouraging results. A delay of 10 ns has been considered in this approach however the system is expected to deliver comparable results with variations in the delay. The variations may include the delay due to arithmetic or logical operations or due to change in the technology and simulation environment. Arithmetic operations need more logic gates and hardware as compared to logical operations thereby leading to larger delays. This issue can further be addressed using minimization methodologies and fast arithmetic circuits since the delay plays a vital role in deciding the clock frequency of the ternary processor. Subprogram overloading provides extensibility and modularity that is highly desirous in digital designing, thus devising an efficient TALU from the perspective of a ternary processor.

4.2 Design And Implementation Of An Efficient Ternary Control Unit (TCU)

Ternary Control Unit (TCU) is the heart and the nerve of theternary processor. This research presents the design of a simplified

control unit for ternary processor. An efficient instruction set comprising of 65 instructions and the required control signals are identified to simulate the functionality of a TCU.

4.2.1 Research Methodology To Design TCU

The steps involved in the hardwired design of the TCU as depicted in figure 4.8 are detailed below:

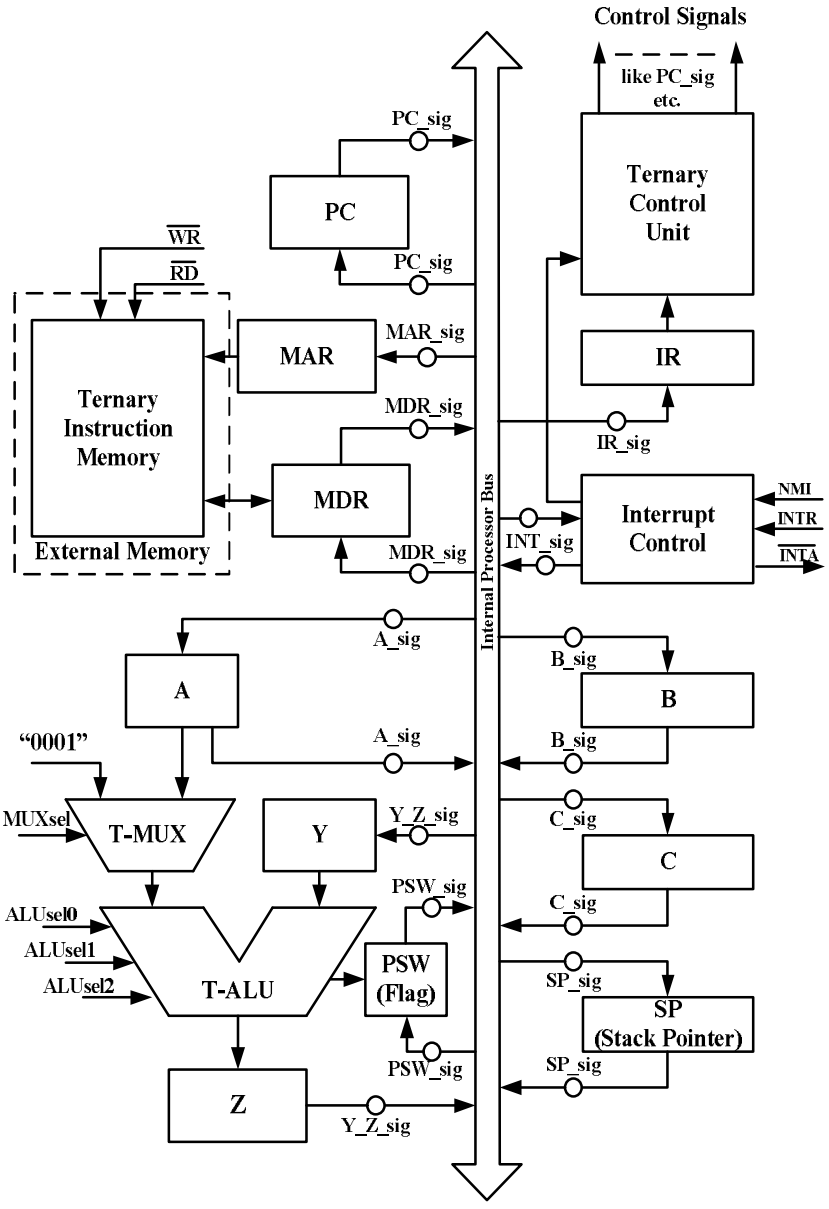


Figure 4.8: Data flow diagram of the ternary processor

Step 1: Specifications of the ternary processor

- Word length: 4 trit
- Logic levels : unbalanced ternary : 0, 1, 2
- Instruction length : 4 trit
- Clock signal : 1 MHz
- Bus organization: Single bus structure
- General purpose registers : 3 (A, B and C)
- Special purpose register: Program Status Word(PSW), Stack Pointer(SP)

Step2: Identifying the instructions, Addressing Modes and assigning the opcode to the instruction

- Addressing modes: register, immediate, direct, implied, relative
- Number of instruction category: 4
- Total number of instructions:65

Table 4.2 describes the instructions belonging to various categories and addressing modes. The chosen instructions and the opcodes assigned to them are also listed in table 4.3. The logical, arithmetic and the data transfer instructions use R_s and R_d, where R_s denotes the source register and R_d denotes the destination register. R_s and R_d can be any of the three general purpose registers. Accumulator (A) is the default destination for the arithmetic instruction.

Table 4.2: The Instruction Set for the design of TCU

Sr. No.	Mnemonic	Operation	Addressing Mode
Logical Instructions			
1	T_ANA Rs	Logical AND	Register
2	T_ORA Rs	Logical OR	Register

3	T_XRA Rs	Logical XOR	Register
4	T_CMP Rs	Complement register	Register
5	T_RAL	Rotate accumulator towards left	Implied
6	T_RAR	Rotate accumulator towards right	Implied
7	T_RLC	Rotate accumulator through carry towards left	Implied
8	T_RRC	Rotate accumulator through carry towards right	Implied
Arithmetic Instructions			
9	T_ADD Rs	ADD without carry	Register
10	T_ADC Rs	ADD with carry	Register
11	T_SUB Rs	Subtract without borrow	Register
12	T_SBB Rs	Subtract with borrow	Register
13	T_ADI data	ADD immediate data	Immediate
14	T_SUI data	Subtract immediate data	Immediate
15	T_ICR Rs	Increment Register	Register
16	T_DCR Rs	Decrement Register	Register
Data transfer Instructions			
17	T_MVI Rd, #data	Move immediate data to accumulator	Immediate
18	T_MOV Rd , Rs	Move Rs into Rd	Register
19	T_LDA addr	Load accumulator with memory contents	Direct
20	T_STA addr	Store accumulator to memory location	Direct
Branch Instructions			
21	T_BUN addr	Unconditional branch	Direct
22	T_BSA addr	Branch and save return address	Direct
23	T_DSZ addr	Decrement Register C and skip if [C] = 0	Direct
24	T_JNC offset	Branch if No carry (i.e. CF = 0)	Relative

25	T_JC offset	Branch if carry (i.e. CF = 1)	Relative
26	T_JNZ offset	Branch if No carry (i.e. ZF = 0)	Relative
27	T_JZ offset	Branch if carry (i.e. ZF = 1)	Relative
Stack operation instructions			
28	CALL Addr.	Subroutine Call	Direct
29	RET	Return from subroutine	Implicit
30	PUSH Rs	Push the contents on the Stack	Register
31	POP Rd	Pop the contents from the Stack	Register

Table 4.3: List of various instructions and the assigned codes

Sr. No.	Mnemonic	OP-Code	Sr. No.	Mnemonic	OP-Code
1	T_ANA A	0001	30	T_SUI data	1010
2	T_ANA B	0002	31	T_ICR A	1011
3	T_ANA C	0010	32	T_ICR B	1012
4	T_ORA A	0011	33	T_ICR C	1020
5	T_ORA B	0012	34	T_DCR A	1021
6	T_ORA C	0020	35	T_DCR B	1022
7	T_XRA A	0021	36	T_DCR C	1100
8	T_XRA B	0022	37	T_MVI A, data	1101
9	T_XRA C	0100	38	T_MVI B, data	1102
10	T_CMP A	0101	39	T_MVI C, data	1110
11	T_CMP B	0102	40	T_MOV A, A	1111
12	T_CMP C	0110	41	T_MOV A, B	1112
13	T_RAL	0111	42	T_MOV A, C	1120
14	T_RAR	0112	43	T_MOV B, A	1121
15	T_RLC	0120	44	T_MOV B, B	1122

16	T_RRC	0121
17	T_ADD A	0122
18	T_ADD B	0200
19	T_ADD C	0201
20	T_ADC A	0202
21	T_ADC B	0210
22	T_ADC C	0211
23	T_SUB A	0212
24	T_SUB B	0220
26	T_SUB C	0221
26	T_SBB A	0222
27	T_SBB B	1000
28	T_SBB C	1001
29	T_ADI data	1002

45	T_MOV B, C	1200
46	T_MOV C, A	1201
47	T_MOV C, B	1202
48	T_MOV C, C	1210
49	T_LDA addr	1211
50	T_STA addr	1212
51	T_BUN addr	1220
52	T_BSA addr	1221
53	T_DSZ addr	1222
54	T_JNC offset	2000
55	T_JC offset	2001
56	T_JNZ offset	2002
57	T_JZ offset	2010

Step3: Instruction memory selection

- External memory interface
- 81x4 memory organization

Step 4: Identification of Control Signals

- Hardwired control unit
- Control signals : 17

- The flow of the data into and out of the register needs to be governed using a control signal. Such a control signal need to be of 'trit' type, where the out operation is performed when the control signal is at logic state '2' and in operation is performed when the control signal is at logic state '1'. The register will remain in idle

state and perform no operation, when the logic state of the control signal is '0'.

- A control signal will specify the read and write operation for memory.
  - When signal is '2' it performs Memory read operation
  - When signal is '1' it performs Memory write operation
  - When signal is '0' it performs No operation

- Three trit control signals are used to select the ALU operation using *'$ALUsel_0$, $ALUsel_1$,$ALUsel_2$. Mux_sel* is the control signal which will select the one of the input to the ternary ALU. Input can be either accumulator or a constant '1'.END signal will specify the end of the instruction and it will reset the two trit step counter.

Table 4.4: Various control signals identified for the TCU

Sr No.	Control signal	Function of the control signal
1.	*PC_sig*	To control in and out operation of the PC register.
2.	*ALUsel0*	First trit (LST) of ALU select.
3.	*ALUsel1*	Second trit of ALU select.
4.	*ALUsel2*	Third trit (MST) of ALU select.
5.	*Muxsel*	To select either Register 'A' or a constant '0001'.
6.	*Y_Z_sig*	To control in and out operation of Y and Z register respectively
7.	*A_sig*	To control in and out operation of the A register.
8.	*B_sig*	To control in and out operation of the B register.
9.	*C_sig*	To control in and out operation of the C register.
10.	*nRD*	To control read operation on memory.
11.	*nWR*	To control write operation from memory.
12.	*MAR_sig*	To control in operation of the MAR register.

13.	*MDR_sig*	To control in and out operation of the MDR register.
14.	*IR_sig*	To control in and out operation of the IR register.
15.	*PSW_sig*	To access the Program Status Word
16.	*SP_sig*	To access the Stack Pointer
17.	*END*	To specify the end of the instruction execution.

Step 5: Exploring the execution of a complete instruction

An instruction execution by default involves obligatory steps of fetching, decoding and it is finally followed by its execution. The fetching and the decoding cycle remain same for all the instructions. The execution of the instruction however, varies and is specific to that instruction and it also depends on the addressing modes. The decoder decodes the contents of instruction register and thus enables the control unit to generate the control signals required for the execution of a particular instruction. It is therefore imperative and necessary to initially identify the required control signals for every instruction. Figure 4.9 shows the data path for fetching the instruction from the instruction memory.

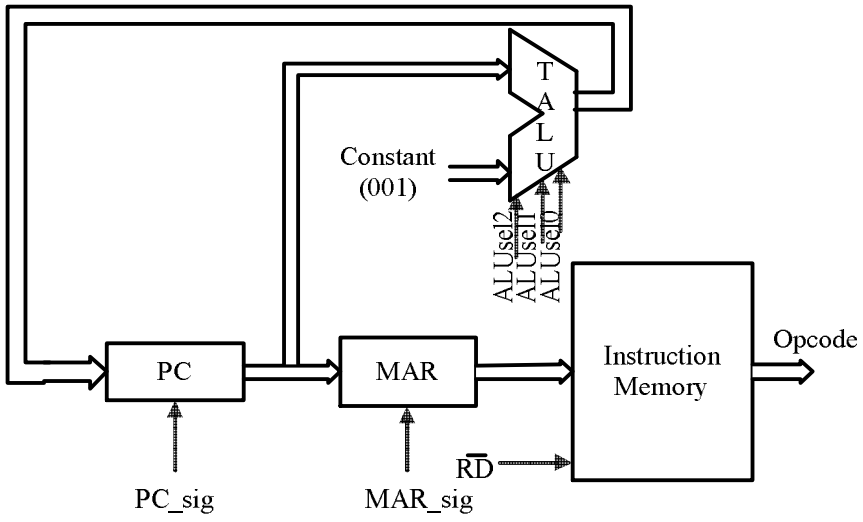


Figure 4.9: Data path for instruction fetch

It may apply to access an operand specified by an instruction.

The Program Counter (PC), controlled by *PC_sig*, generates the address for instruction fetch cycle. After the assertion of *MAR_sig*, the Memory Address Register (MAR), latches the current address pointed by PC. The PC must be incremented to point at the address of the next following instruction or operand. As indicated in Figure 4.9, a constant of '0001' is added to the present address of the PC using ALU. The ALU is configured to perform addition using the *ALUsel* control signal of ALU.

Table 4.5 describes the control sequence for the execution of the instruction fetch phase. The fetch and decode phase are common to all the instructions and have therefore been generalized. The required control signals and the sequence of operation are detailed above. The control signals as clearly seen take ternary values and are thus able to dual operations. When *PC_sig*is 1, write operation is performed and when *PC_sig*is 2, read operation is performed. Logic state '0' of *PC_sig* indicates its idle state. Machine cycle consists of many clock periods called T-states. Depending on the operation to be performed each instruction requires varying number of machine cycle.

Figure 4.10 illustrates the timing diagram for instruction '*T_MVI A, #data'*, which loads the accumulator with an immediate ternary data. Two machine cycles (Fetch and Memory Read) are utilized for the execution of the instruction. In state T_0 of the memory is provided with the address of the instruction, leaving the data line idle. As already represented in figure 4.9, the address must be incremented by 1, which is accomplished in state T_1. At the end of T_1, the control unit asserts the read signal that makes the data in memory available on the data bus, which is the opcode of instruction. The states T_0, T_1 and T_2 thus represent the fetch cycle of instruction execution.

Table 4.5: Control sequence for instruction fetch and decode

T-States	Control Signals
T0	*PC_sig=2; MAR_sig=1; Y_Z_sig=1; MUXsel=2; ALUsel=000*
T1	*PC_sig=1; Y_Z_sig=2; nRD=0*
T2	*IR_sig=1; MDR_sig=2*

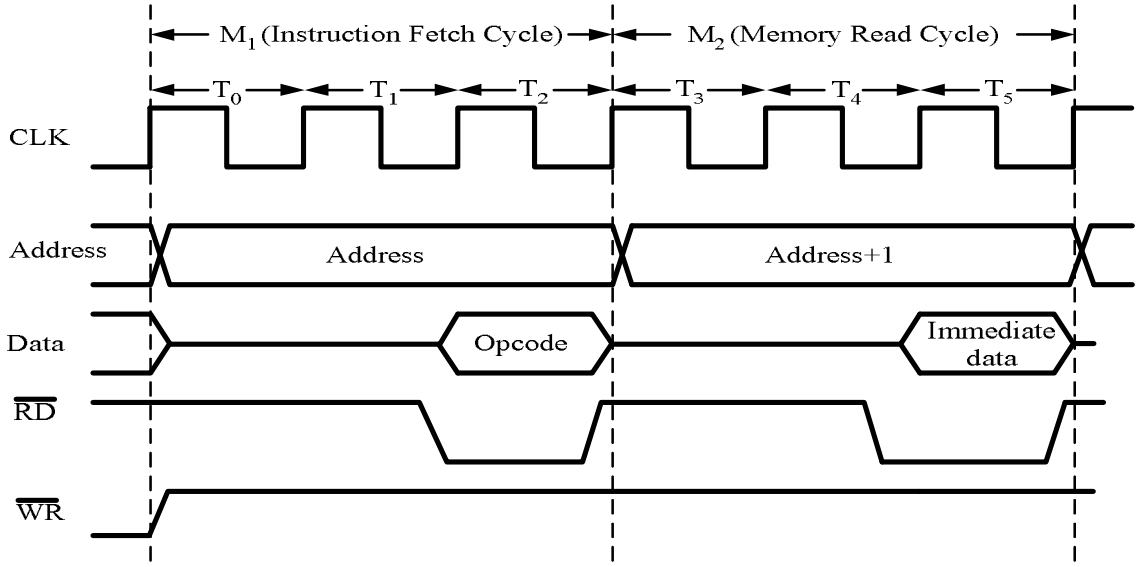


Figure 4.10: Timing diagram for instruction T_MVI A, #data

In state T_3, the address of the operand is provided to the memory. Similar to state T_1, in state T_4 address is incremented and read signal is asserted. In state T_5, the immediate data is read from the memory and loaded in the accumulator, which is the operand. The CU generates the corresponding control signals as indicated in Table 4.4, for the states T_3, T_4 and T_5, which represents the execution phase of the instruction.

Table 4.6:Control sequence for'T_MVI A, #data'

T-States	Control Signals
T3	*PC_sig=2; MAR_sig=1; Y_Z_sig=1; MUXsel=2; ALUsel=000*
T4	*PC_sig=1; Y_Z_sig=2; nRD=0*
T5	*A_sig=1; MDR_sig=2;END*

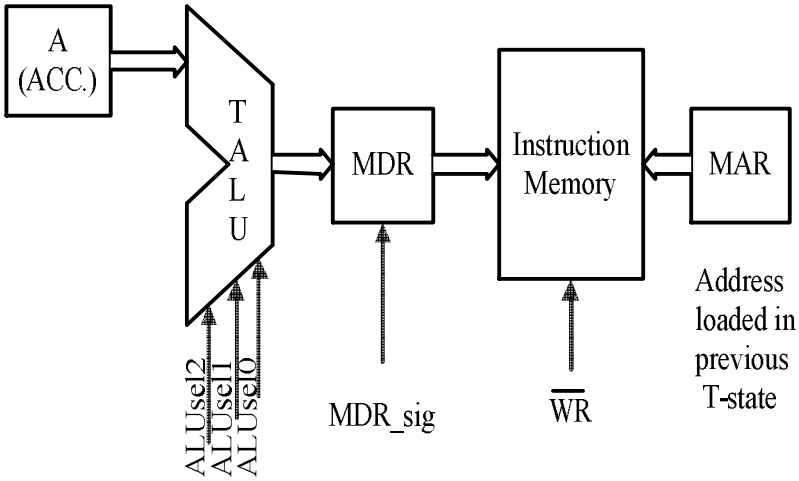


Figure 4.11:Data path for memory write operation

Some instructions, like *T_STA* involve a memory write operation. The data path in such a case differs from Memory read operation and the execution phase requires more number of T states. Figure 4.11 represents the data path for memory write operation, where MDR and MAR are the Memory Data Register and Memory Address Register respectively. The accumulator contents are loaded in the MDR through ALU, by configuring ALU in transfer mode. The control signal *MDR_sig* is in state '1' to facilitate the write operation. Asserting the active low, write signal further loads the contents in the Memory location pointed by MAR. The previous T state must load the MAR with the expected address as provided in the instruction.

Figure 4.12 represents the timing diagram for the execution of *'T_STA addr'*. As indicated, this instructions demands additional machine cycle for the Memory write operation. The states, T_0 to T_2 represent the fetch cycle and the instruction execution cycle which begins at T_3 and continues until state T_7. The destination address, i.e. the location in memory where the contents of accumulator are to be stored, is accessed in states T_3, T_4 and T_5. In state T_6, the accessed address is provided on the address bus, which is further buffered in MAR. At the

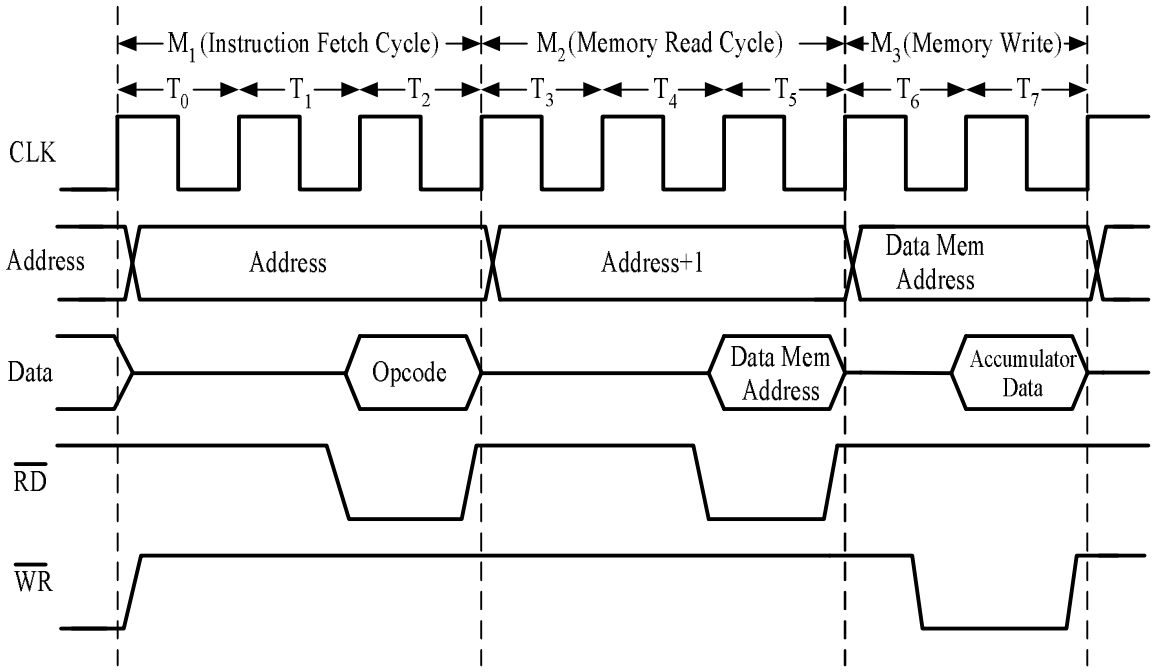


Figure 4.12: Timing diagram for instruction T_STA addr

end of T_6, write signal is asserted which enables the memory write operation for storing the contents of the accumulator in the memory location. The CU generates the corresponding control signals as indicated in Table 4.7, for the states T_3, T_4 and T_5, which represent the execution phase of the instruction.

Table 4.7: Control sequence for the execution of instruction 'T_STA addr'

T-States	**Control Signals**
T3	*PC_sig=2; MAR_sig=1; Y_Z_sig=1; MUXsel=2; ALUsel=000*
T4	*PC_sig=1; Y_Z_sig=2; nRD=0*
T5	*Y_Z_sig=1; MDR_sig=2; ALUsel=010*
T6	*Y_Z_sig=2; MAR_sig=1; nWR*
T7	*MUXsel=1; ALUsel=020; Y_Z_sig=2; MDR_sig=1; END*

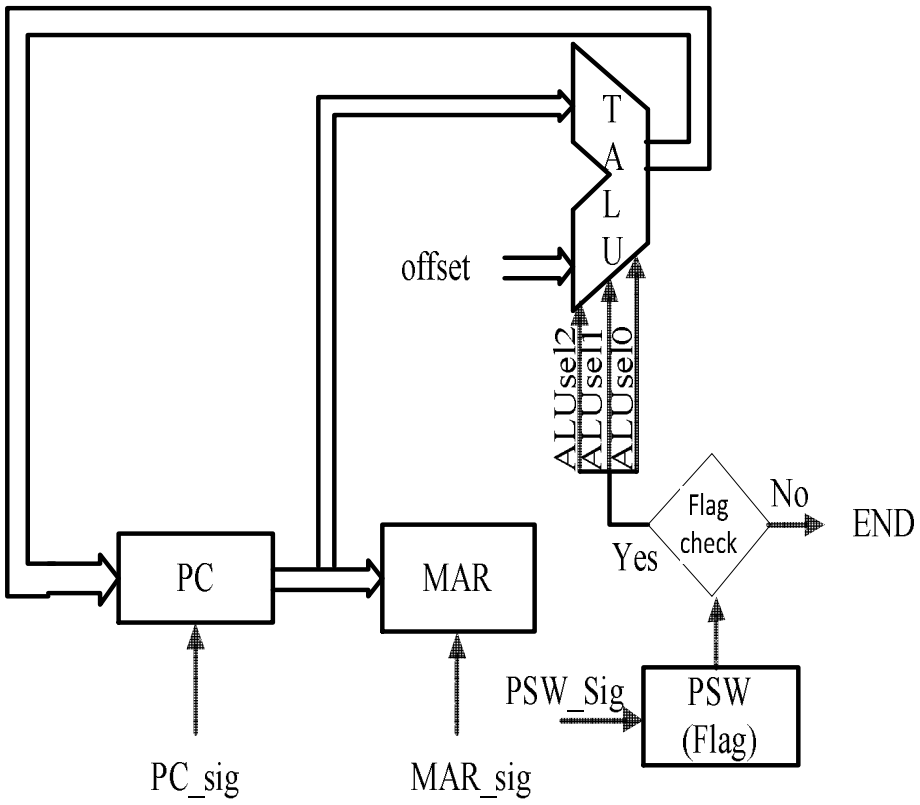


Figure4.13: Data path for conditional branch instruction

Figure 4.13 represents a general data path for conditional branch instruction, i.e. Branch if the condition of the program status word (flag) is satisfied. To execute such an instruction, PSW_sig is asserted to access the PSW register. Upon the fulfillment of the condition the offset is added to the current address pointed by the PC so as to locate the destination branching address. '*ALUsel'* lines are asserted to configure the ALU in the addition mode. If the condition is not satisfied, the instruction execution is terminated by using END control signal. Control sequence for the execution of instruction 'JNC offset' is represented in Table 4.8. The number of T states required for the execution of the Branch Instruction depends upon the fulfillment of the condition.

The instruction set also considers the PUSH and POP instructions related to Stack. Stack Pointer (SP) points the stack memory and

initialized using MVI SP, #loc instruction. For PUSH operation stack pointer is decremented initially and the contents of the register are pushed on the memory pointed by SP. On the contrary, for POP initially the contents are read from the location pointed by SP and then stack pointer increments. Table 4.9 and Table 4.10 describe the control sequence for the execution of these instructions.

Table 4.8: Control sequence for the execution of instruction 'JNC offset'

T-States	Control Signals
T3	*PC_sig=2; MAR_sig=1; Y_Z_sig=1; MUXsel=2; ALUsel=000*
T4	*PC_sig=1; Y_Z_sig=2; nRD=0; PSW_Sig = 2*
T5	*A_sig=1; MDR_sig=2; MUXsel=1; ALUsel=000; if (CF = '1') then END*
T6	*Y_Z_sig=2; PC_sig=1; END*

Table 4.9: Control sequence for the execution of instruction 'PUSH A offset'

T-States	Control Signals
T3	SP_sig = 2, Y_Z_sig = 1, ALUsel = 022
T4	Y_Z_sig = 2, SP_Sig = 1, MAR_sig = 1
T5	MUXsel =1, ALUsel = 010, nWR=0
T6	Y_Z_sig = 2, MDR_sig = 1, END

Table 4.10: Control sequence for the execution of instruction 'POP A'

T-States	Control Signals
T3	SP_sig = 2, Y_Z_sig = 1, MAR_sig = 1, nRD=0
T4	MDR_sig = 2, A_sig, ALUsel = 021
T5	Y_Z_sig = 2, SP_sig = 1, END

Step 6: Deriving the logical equations for control signals:

Execution of the instructions comprises of various T states. Every T state has a different set of control signals. It is therefore necessary to derive a logic function for the generation of each control signal. The control sequence of instruction execution is utilized for deriving the logic function for the various control signals. Table 4.11 indicates the logic functions for the generation of few control signals like *PC_sig*, *MAR_sig*, *MDR_sig*.

Step 7: Modeling of the control unit using VHDL

A user defined *'VHDL package'* for ternary system that includes ternary data type *'TERNARY_LOGIC'* is developed and additionally a '*TERNARY_LOGIC_VECTOR'*data type has also been declared to accommodate the ternary arrays. The 'trit' data type can take one of the three values (0, 1, 2). The designed instruction set includes various arithmetic and logical operations, therefore corresponding functions are also included in the package to perform addition, subtraction, logical AND, OR, XOR and other operations.

The fundamental blocks in a processor that includes ALU and memory, as depicted in figure1are modeled in VHDL. The ternary ALU is designed to perform the various operations which are selected using the combination of 3-trit select lines. An 81 x 4 ternary memory is devised with 4 trit address lines and 4 trit data bus to store the program.

Table 4.11:Logical equations for sample control signals

Control Signals	**Equation**
PC_sig	*T0.I2 +T1.I1 +T3.I28. I29.I36.I37.I38.I48.I49.2 +T4. I28. I29.I36.I37.I38.I48.I49.1*
MAR_sig	*T0. I1+T3. I28. I29.I36.I37.I38.I48.I49.1+T6.I48.1*
MDR_sig	*T2.I2+T5. I28. I29.I36.I37.I38.I48.I49.2+T6. I48.2+ T6.I49.1*

Figure4.14 illustrates the fundamental blocks of a hard wired control unit which are responsible to generate the identified control signals, indicated in Table 4.4.Each step of the control signal is driven by a ternary clock. The step counter keeps a track of the T-states and step decoder further activates the corresponding T-state signal (T_0, T_1 …T_8). Instruction decoder decodes the op-code as specified by the instruction loaded in the instruction register (IR). In the presented design, 4:81 instruction decoder is used to accommodate 65 instructions corresponding to the 4-trit op-code. The input signals to the encoder ,I_n where n= 0 to 56 and T_m, where m= 0 to 8, are combined to generate the control signals for the active T state of the respective instruction. In the ternary encoder, different control signals are generated using ternary gates. A complete Ternary Control Unit (TCU) is

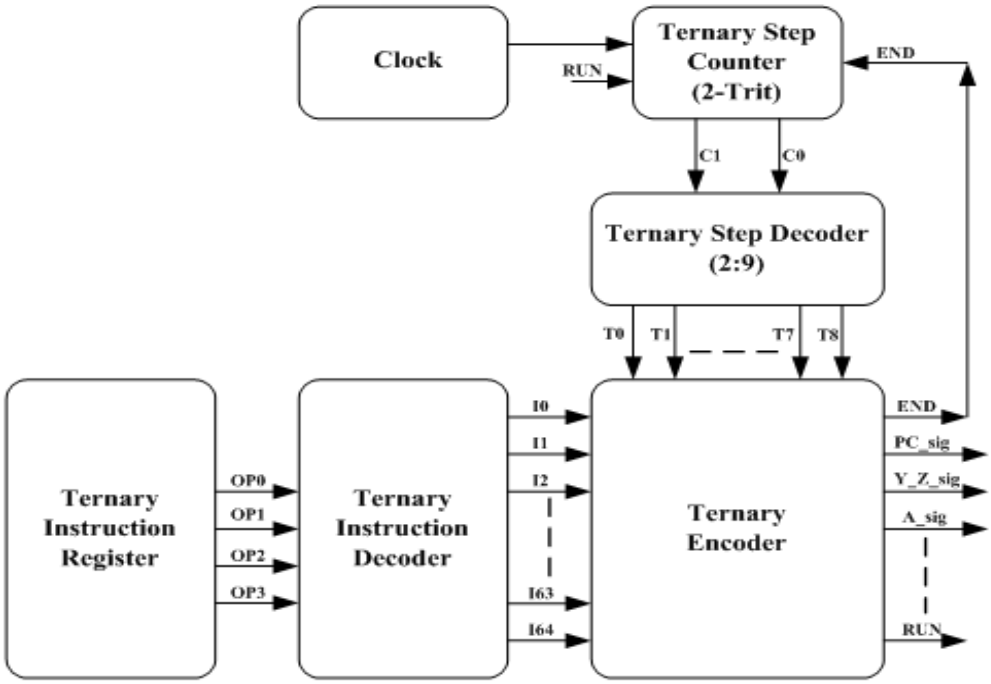


Figure 4.14: The fundamental blocks in the TCU

modeled using VHDL. A gate level design is used for implementing vectored TALU and TCU.

4.2.2 Simulation Results

The control unit designed for a ternary processor is functionally verified using Xilinx ISE 14.2 version, ModelSim 6.5. Figure 4.14 shows the simulation result of the generation of control signals for execution of instruction *T_MVI A,#nn*. The instruction transfers the immediate source operand to the accumulator. TCU unit provides control signal at each ternary clock edge according to the input from instruction decoder and step counter.

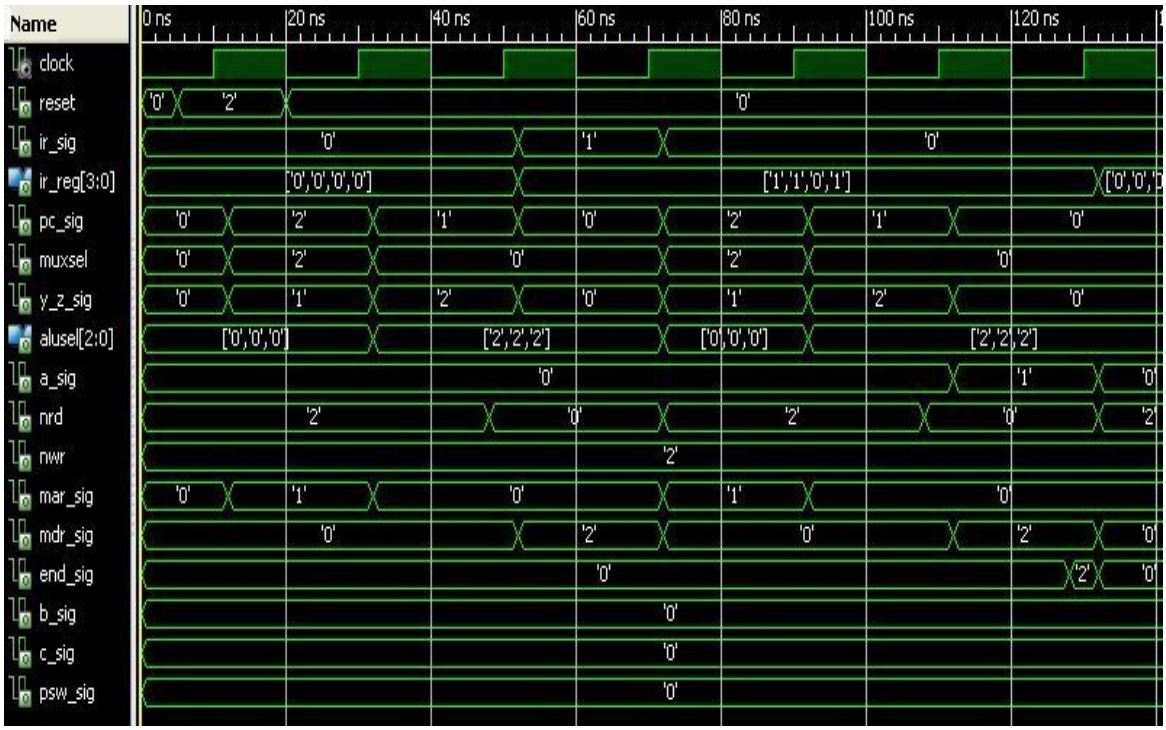


Fig 4.14 :Simulation results of an instruction (T_MVI A,#nn)

In the state T0, the control signals *PC_sig* and *MAR_sig* are generated to govern the loading of MAR with the contents of PC through the internal bus. The PC is incremented in T_1 state so that it points the address of the next instruction or operand. The opcode value '1101' is loaded into the instruction register in T_2 T-state using the control signals *IR_sig* and *MDR_sig*. The memory is accessed for the source operand of the instruction in T_3 state. *PC_sig*, *MAR_sig*, *nRD* coordinate this operation and are therefore appropriately generated as indicated in the simulation results. The PC points to the next instruction address in the T_4 state. The source operand is moved to the accumulator in T_5 state as sequenced by the activation of *MDR_sig* and *A_sig*. The operation comes to an end with the generation of *end_sig*. The step counter is reset after this operation to initiate the next instruction as pointed by the PC. On similar grounds, the control sequence for the instructions *T_STA* address and *T_JNC* offset are

verified and represented in figure 4.15 and figure 4.16. As indicated, in figure 4.13 the control signal *PSW_sig* is asserted only during the execution of the branch instruction. Figure 4.17 and figure 4.18 depict the simulation results for the PUSH and the POP instructions.

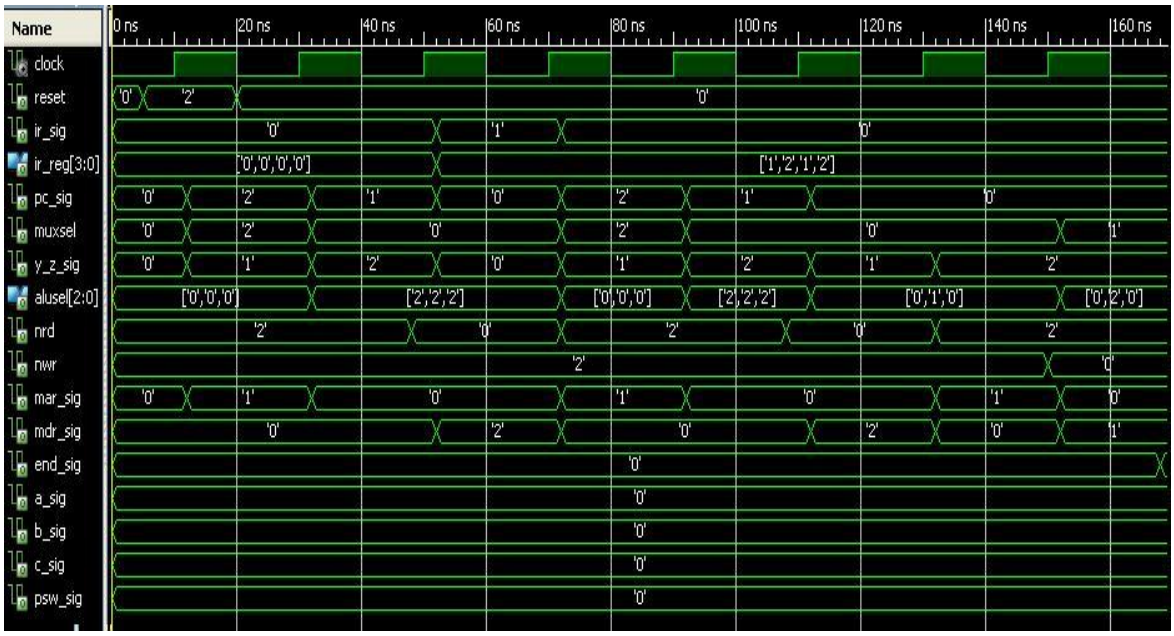


Figure 4.15:Simulation results of an instruction (T_STA address)

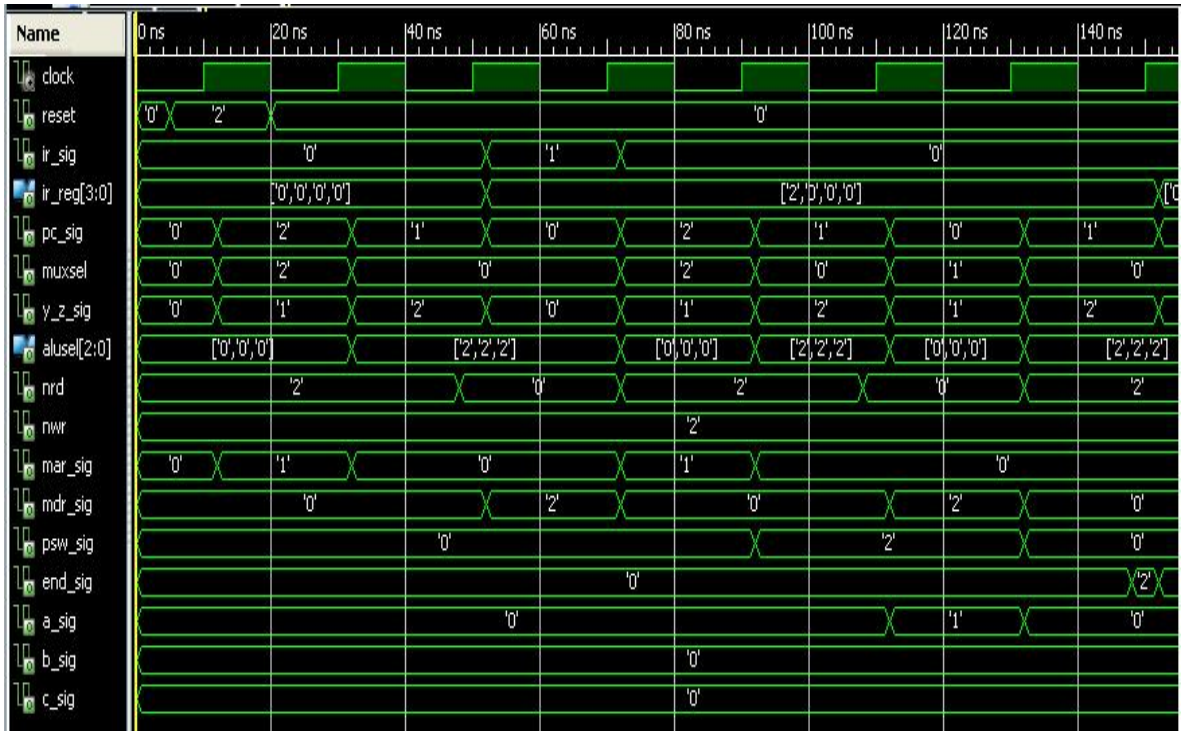


Figure 4.16:Simulation results of an instruction (T_JNC offset)

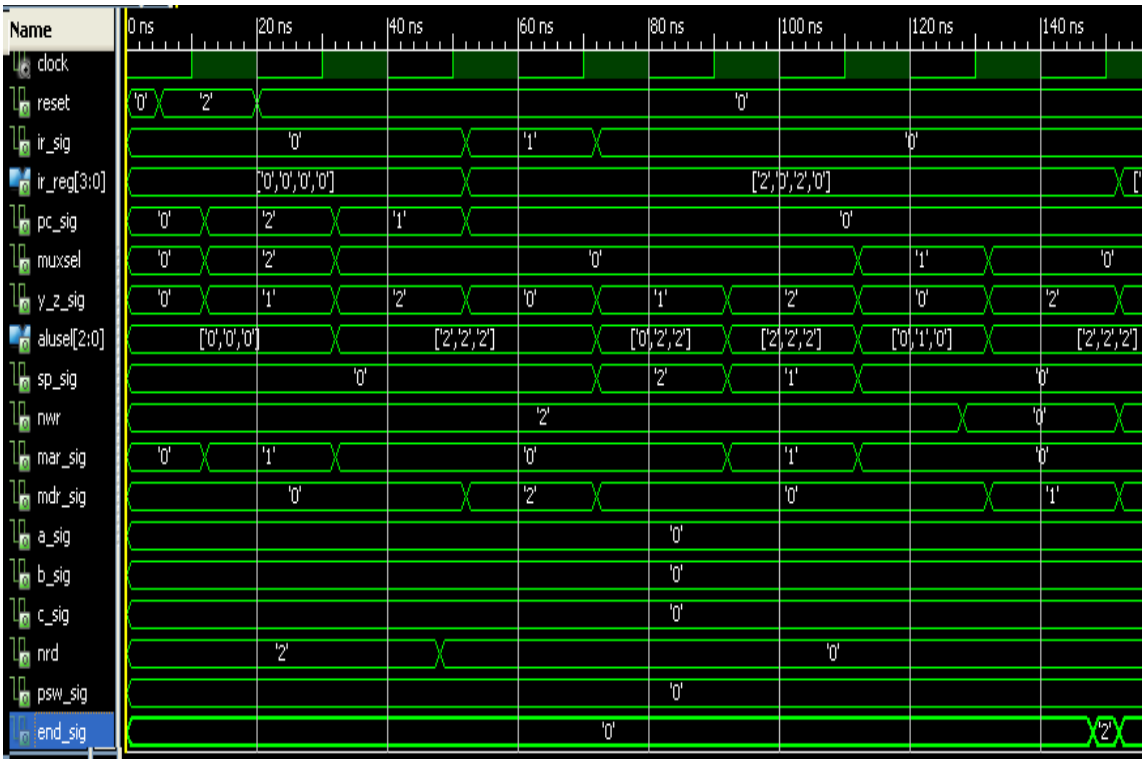


Figure4.17 :Simulation results of an instruction (PUSH A)

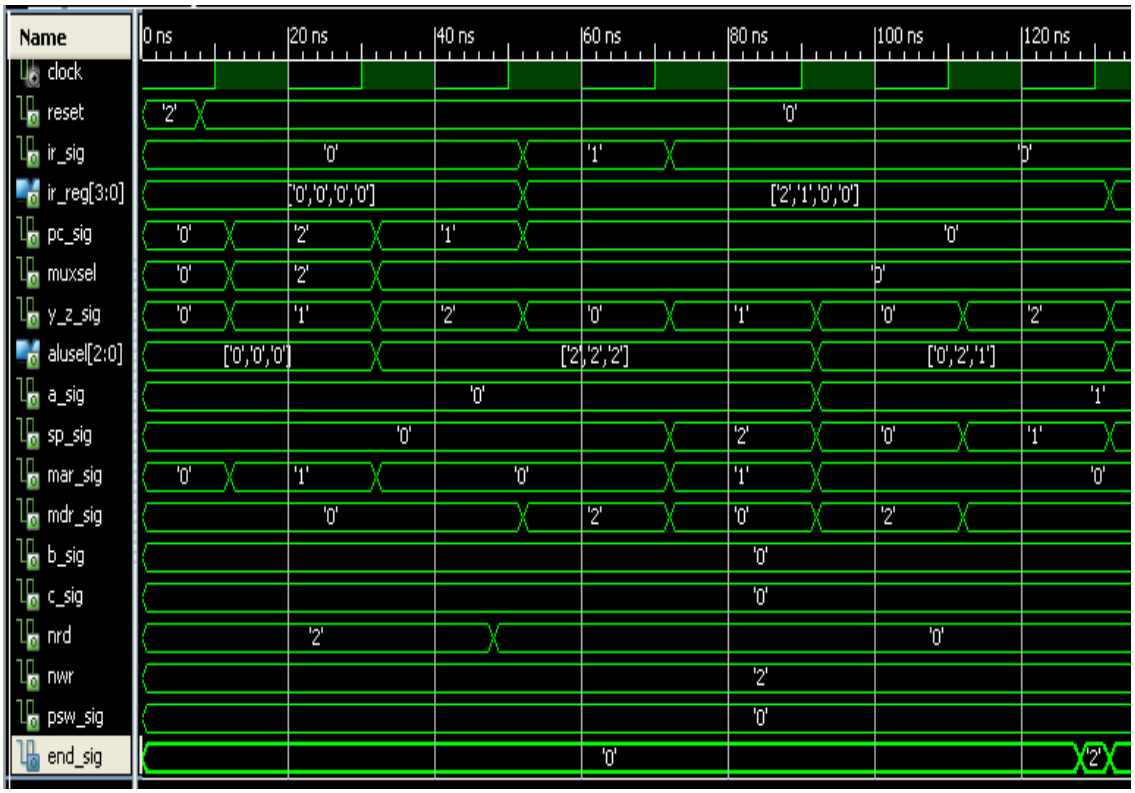


Figure 4.18: Simulation results of an instruction (POP A)

The functionality of the designed TCU was extensively analyzed using the instruction set including various addressing modes. T-states required for the execution of any instruction varies according to its corresponding addressing mode. Table 4.12 compares the number of T states for the execution of the instructions belonging to the various addressing modes. As expected, the immediate, direct, absolute and relative addressing modes require more number of T states due to increase in the memory referencing.

Table 4.12:Comparison of the T states in every addressing mode

Addressing Mode	T-state required
Register Addressing Mode	5
Implied Addressing Mode	5
Immediate Addressing Mode	7/6
Direct Addressing Mode	7
Relative Addressing Mode	5/6

4.2.3 Discussion

This research presents an efficient design of TCU for a ternary processor using Very-High-Speed Integrated Circuits, VHSIC Hardware Description Language (VHDL), which is effectively the nerve centre of a processor that plays a vital role in generating the appropriate control signals and synchronizing all the operations. The functionality of the designed TCU is verified using sixty five instructions belonging to various addressing modes. The control signals required for the execution of the instructions are identified and further modeled using VHDL. This research shows the potential of VHDL modeling and simulation that can be applied to TCU. The extensive simulation results of the designed TCU signify encouraging results that will pave the path for further developments in ternary processors.

4.3 In the Nutshell

TALU and TCU, both are the fundamental units of any processor. The task of effectively designing the TALU and TCU for a ternary processor has received comparatively less attention by the researchers and to the best of our knowledge, meager work is reported in the literature addressing this concern. With effective MIFG based realization of the ternary combinational and sequential circuits, it is necessary to further extend its functionality and simulate the modules from the perspective of a ternary processor.

This research presents simulation and timing analysis of the 4-trit vectored TALU. Altogether 18 operations are implemented in the TALU developed from the perspective of ternary processor. The implementation of subprogram overloading feature in the presented TALU makes its design unique, flexible and portable for further extension.

The control unit is the heart of the processor. This research presents a hardwired design for an efficient TCU. The outputs of the TCU are the control signals required for the sequencing operations and the coordination of the entire processor. The designed TCU makes use of relatively less number of control signals as compared to binary logic. This is because a binary control signal offers only two logic levels to control the operations. It must be emphasized that the design exploits the multi valued ternary logic. Only one control signal *'Y_Zsig'* coordinates both Z and Y registers. Moreover, *'PC_sig'* is used to control the in and out operations of a program counter. The designed TCU thus makes wise assignment of the control signals and is therefore optimized. The VHDL modeling of the designed control unit is simulated using an instruction set of 65 instructions to ensure that the TCU is functional and operated as expected. The designed TCU can operate at speed of 1MHz when subjected to gate delay of 10ns.

CHAPTER 5

RESULT ANALYSIS

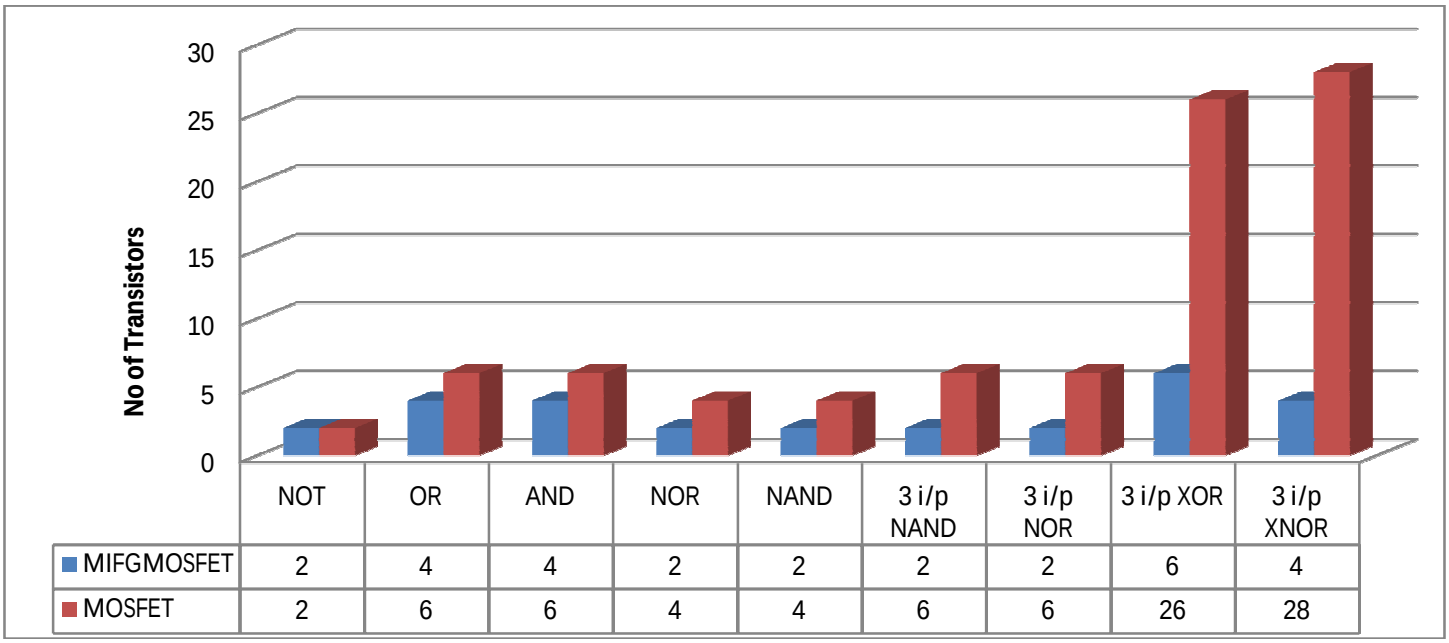
Despite the potential advantages of ternary logic over the binary logic, realization of an efficient, realistic and a practical ternary processor is still a thrust area of research. The focus of this research revolves around exploring a switching device that supports ternary logic system and simulation and testing of the fundamental modules of ternary processor.

The investigation of the results derived using the research methodology adopted in this investigation includes the analysis of:

- MIFG Based Realization
- The simulation and synthesis results of various ternary circuits

5.1 Analysis of MIFG Based Realization of Binary Circuits

MIFG has proved to be an intelligent choice for the realization of the binary gates. The designed binary NOT, NAND and NOR gates can be further used to implement the AND, OR, EXOR and XNOR gates. PDP of MIFG-MOSFET gates are acceptable and it not only ensures good functionality but good improvement in the performance parameters is also obtained. Moreover, substantial reduction in the total number of transistors in the design is found to be more than 50%. Figure 5.1 compares the MIFGMOSFET and the traditional CMOS implement, which directly proves the superiority of using MIFG for the realization of the binary gates. MIFG based binary gates play a crucial role in efficient realization of the ternary circuits.



	NOT	OR	AND	NOR	NAND	3 i/p NAND	3 i/p NOR	3 i/p XOR	3 i/p XNOR
MIFGMOSFET	2	4	4	2	2	2	2	6	4
MOSFET	2	6	6	4	4	6	6	26	28

Figure 5.1: Comparison of the MIFGMOS and CMOS based approach for the implementations of the binary gates in terms of the circuit element count.

5.2 Analysis of MIFG Based Ternary Gates

This research presents a MIFG based standard ternary inverter (STI). Extensive performance analysis of the designed STI is performed. Figure 5.2 depicts the Voltage Transfer Curve (VTC) of the STI. Three states corresponding to logic level 0, 1 and 2 are clearly seen. Ternary logic has four different noise margins as described in [13]. The obtained VTC curve is used to further calculate the noise margins. The obtained results for the Noise Margin and Rise/ Fall time are summarized in the table 5.1 and 5.2 respectively. As indicated in table 5.2, the transition time of the MIFGMOS transistor based STI is less than the other reported approaches in [9,13]. The comparison with the state of art methods as detailed in table 5.1 and 5.2 showcases the effectiveness and advantages of replacing the conventional MOSFET inverter with the MIFGMOS for the realization of STI.

Table 5.1: Noise Margin of STI

NM_0	0.60V
NM_1^-	0.92V
NM_1^+	0.73V
NM_2	0.93V

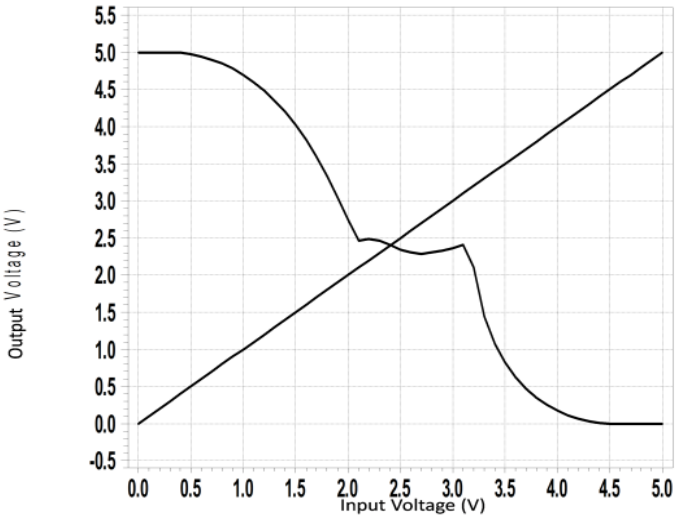


Figure 5.2: VTC of STI

Table 5.2: Rise/ Fall time of the MIFG based STI

Transition logic to logic	**Rise / Fall time**		
	[9] *Bala P C et. al.*	**[13]** *Supriya et. al.*	**MIFG based approach**
1-2	12 ns	11.18 ps	**5.09 ps**
2-1	12 ns	11.18 ps	**5.20 ps**
1-0	20ns	11.18 ps	**6.84 ps**
0-1	20 ns	11.18 ps	**4.54 ps**
2-0	20 ns	13.43 ps	**10.43 ps**
0-2	20 ns	13.41 ps	**10.43 ps**

This research also presents a novel hybrid approach based on MIFGMOS technology for the realization of the ternary gates. The designs based on hybrid combination of devices of two input TNAND and TNOR gates are detailed. The designed TNAND and TNOR gates along with MIFGMOS transistor based T-inverter is further used to design TAND, TOR, TXOR and TXNOR gates. An extensive simulation of all the designed gates is carried out using TSPICE circuit simulator. The results demonstrate expected functionality of the designed hybrid gates and an additional improvement in the performance parameters is also achieved.

The earlier reported CMOS technique for the implementation of ternary gates uses an additional power supply and passive components to obtain the intermediate state i.e. logic state '1' [6, 50]. This is because, in such circuits CMOS operates only in ON and OFF states. The novel approach however eliminates the need of additional power supply and components to achieve the intermediate state. The weighted sum of the input voltages at floating gate provides the flexibility to drive the circuit in ON, OFF and intermediate state. This is significant improvement as compared to the earlier CMOS designs [6,50,38].

The operating voltage in the hybrid approach is selected to be 5 V, which is expected to provide a better fan-in when further used in the ternary combinational and sequential circuits. As already indicated in the PDP graphs, the functionality of the designed gates was verified for various frequencies (500 KHz to 5 MHz) and various loads (1pF to 10 pF). Apparent advantage of using 5V as the operating voltage is the higher noise margins. The literature reports the noise margin of 50 mV for the operating voltage of 500 mV [6]. The noise margins of the designed gates, as summarized in table 5.1, are quite higher than the

reported values.

Table 5.3 presents the comparison of the number of elements used in the MIFG based approach with earlier reported literature. The hybrid approach presented in this research has achieved good reduction in the circuit element count. This reduction will further be more significant when building ternary combinational and sequential circuits.

The simulation results and the comparison table 5.3 confirms the authenticity of the novel hybrid MIFGMOS transistor based method as well as the superiority of the designed ternary circuits specifically in terms of the circuit element count and performance parameters like PDP and rise /fall time in comparison with the other state-of-the-art ternary circuits. The figure 5.3 to figure 5.7 depicts the PDP as obtained for the designed gates. The designed gates are rigorously analyzed to calculate the PDP at various frequencies ranging from 500 KHz to 5 MHz and at various loads of 1pf to 10 pf. As expected, the PDP increases with increase in load and for a specific load, the PDP remains constant inspite of large variations in frequency. The designed MIFG based gates deliver promising performance.

Table 5.3: Comparison of number of circuit elements for the implementation of ternary gates

Sr. No.	**Designed Ternary Circuits**	**CNTFET [1] *Sheng et. al*.**	**QDGFET [13] *Supriyaet. al.***	**Hybrid (MIFG-MOS) Approach**
1.	T-INV (STI)	06	03	**02**
2.	T -NAND	10	04	**03**
3.	T-NOR	10	04	**03**
4.	T-AND	16	07	**05**
5.	T-OR	16	07	**05**

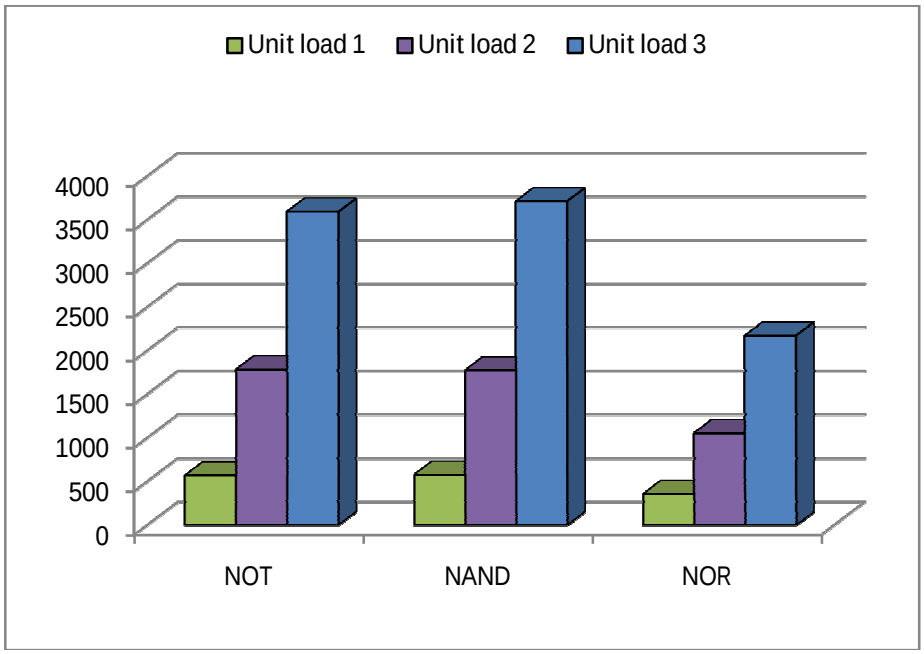


Figure 5.3: PDP of ternary gates

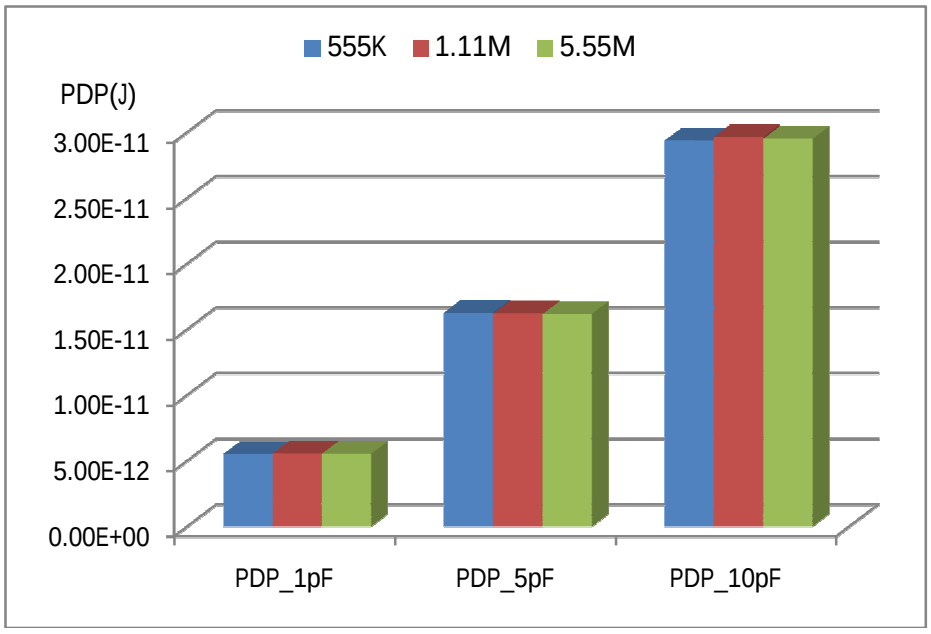


Figure. 5.4: PDP of TNAND for different capacitive load and frequencies

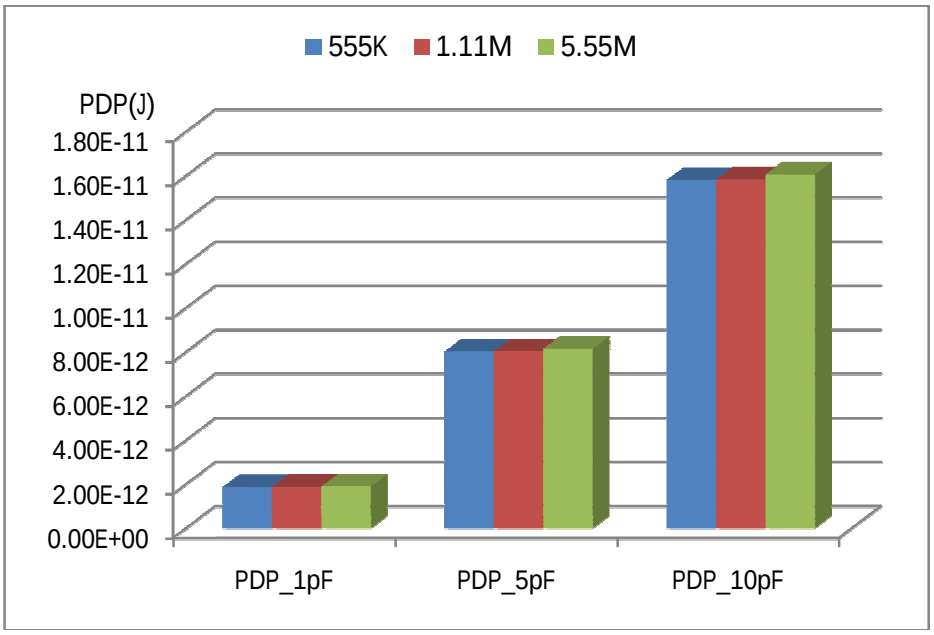


Figure 5.5: PDP product of TNOR for different capacitive load and frequencies

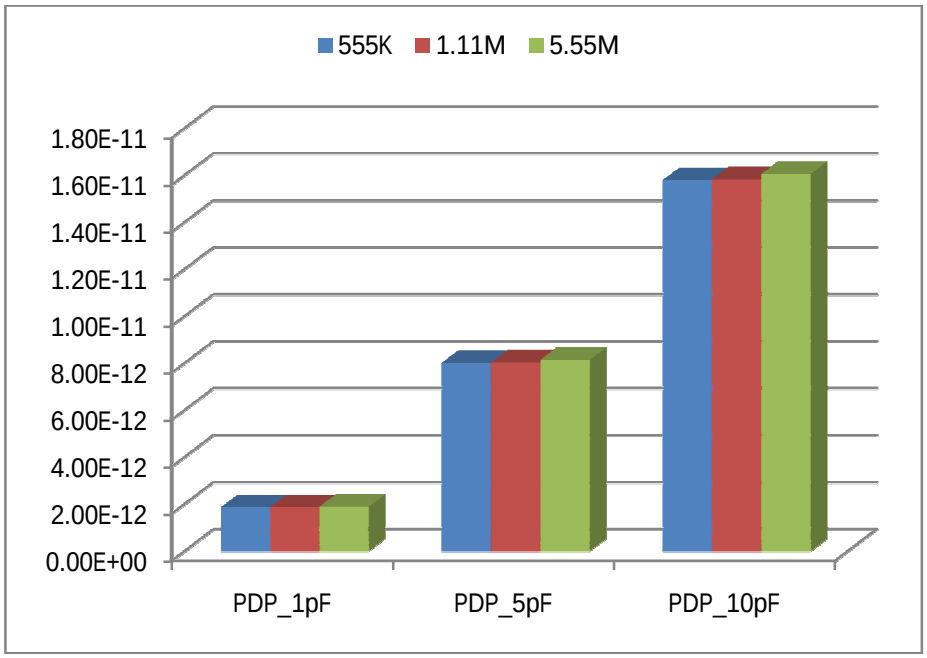


Figure 5.6: PDP of TAND for different capacitive load and frequencies

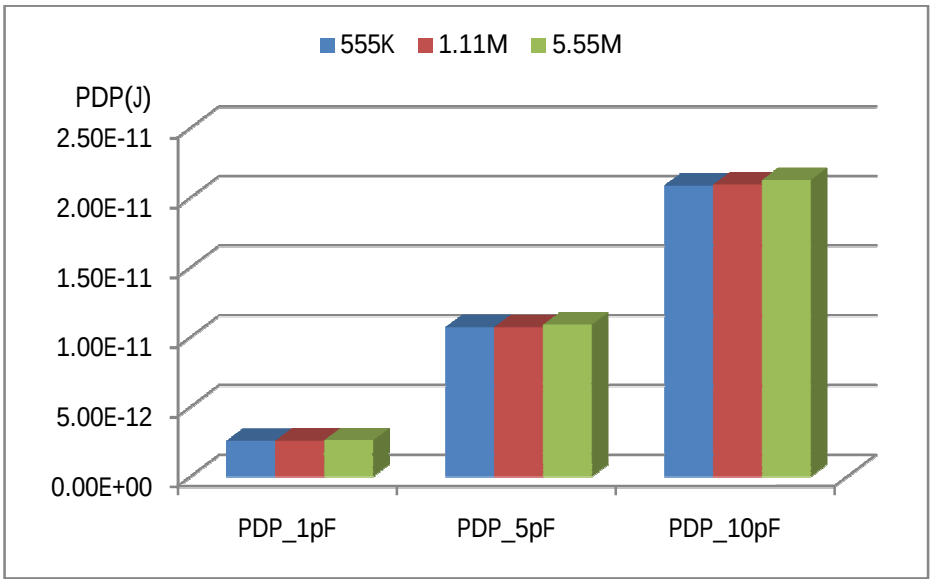


Figure 5.7: PDP of TOR for different capacitive load and frequencies

5.2.1 Performance analysis of the MIFG based TALU

This research extends the implementation of the ternary gates to presents an efficient hybrid approach based on combination of MIFGMOS transistor and conventional MOSFET for the realization of the Ternary Arithmetic and Logic Unit (TALU).

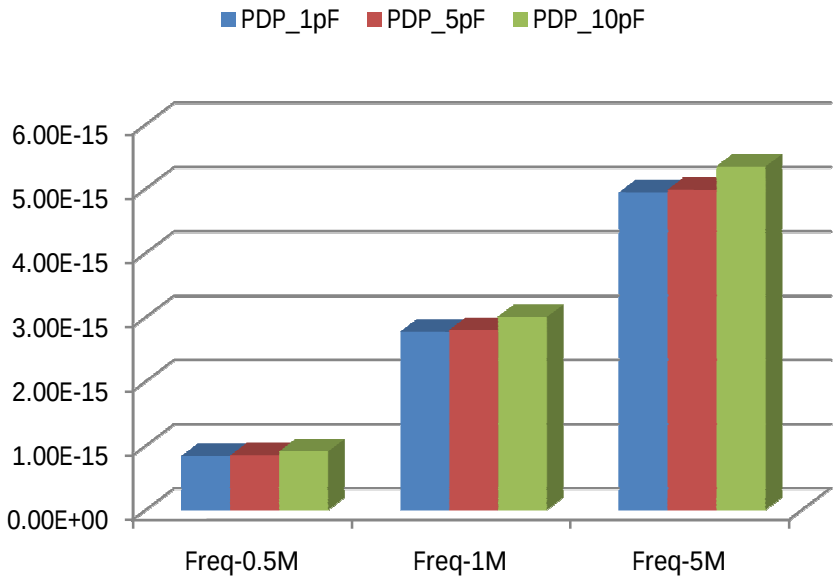
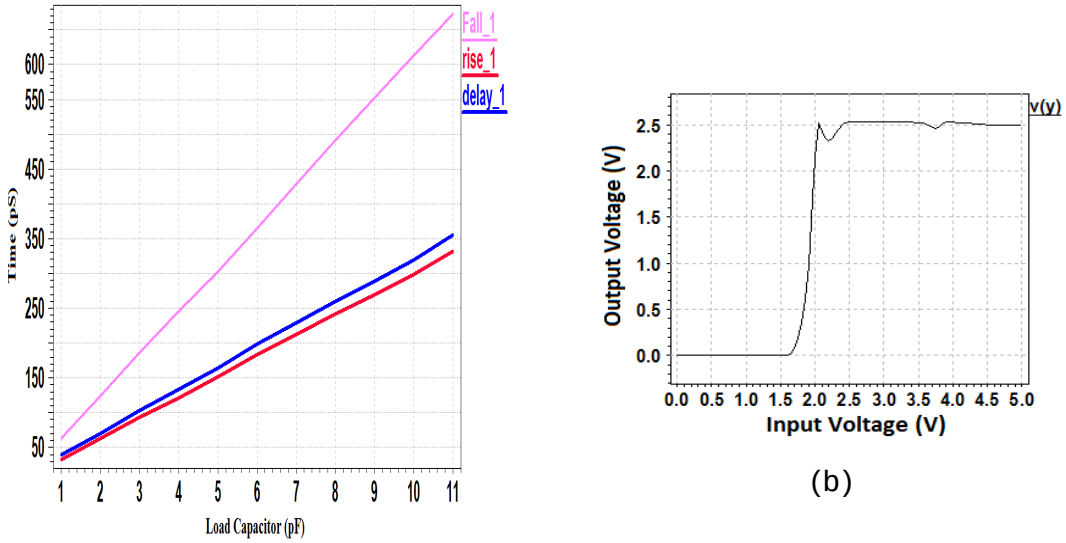


Figure 5.8: Performance analysis of the modified ternary decoder

The MIFMOS transistor based binary gates and hybrid MIFGMOS transistor based ternary gates are initially designed and effectively simulated. A modified design of ternary decoder is presented using the devised MIFGMOS transistor based binary NOR gate that leads to reduction in circuit element count. The PDP analysis different capacitive load and frequencies as depicted in figure 5.8 demonstrate encouraging results.

A novel Ternary Level Shifter (TLS) that has received meager attention in the reported literature is also presented in this paper. It exploits the controllability and tunability of the MIFGMOS transistor to achieve an intermediate voltage level (logic level '1') and thereby the desired functionality of the level shifter. Moreover the need of passive components and an additional power supply ($V_{DD}/2$) is completely eliminated leading to considerable reduction in the power. Figure. 5.9(a) illustrating depicts the performance analysis of the designed TLS depicting the rise/ fall time and the delay with respect to the variation in load capacitance. The VTC curve is also plotted in figure 5.9 (b) to calculate the noise Margins of TLS as tabulated in Table 3.8



(a) (b)

Figure 5.9: (a) Performance analysis of the TLS depicting the rise/ fall time and the delay w.r.t the variation in load capacitance. (b) VTC curve and the noise margins

The MIFG based combinational circuits devised in this research are also analyzed to validate its performance and compare it with the state of the art methods in terms of the circuit elements and the transient responses.

Transient response of the MIFGMOS THA using both ternary logic gates and binary logic gates is shown in figure 5.10 and is further compared with the transient delays of the various reported approaches. The MIFG based hybrid THA achieves significant reduction in circuit element count and showcases improved performance parameters.

Table 5.4: Noise margin of TLS

NM1	300 mV
NM0	1.57 V

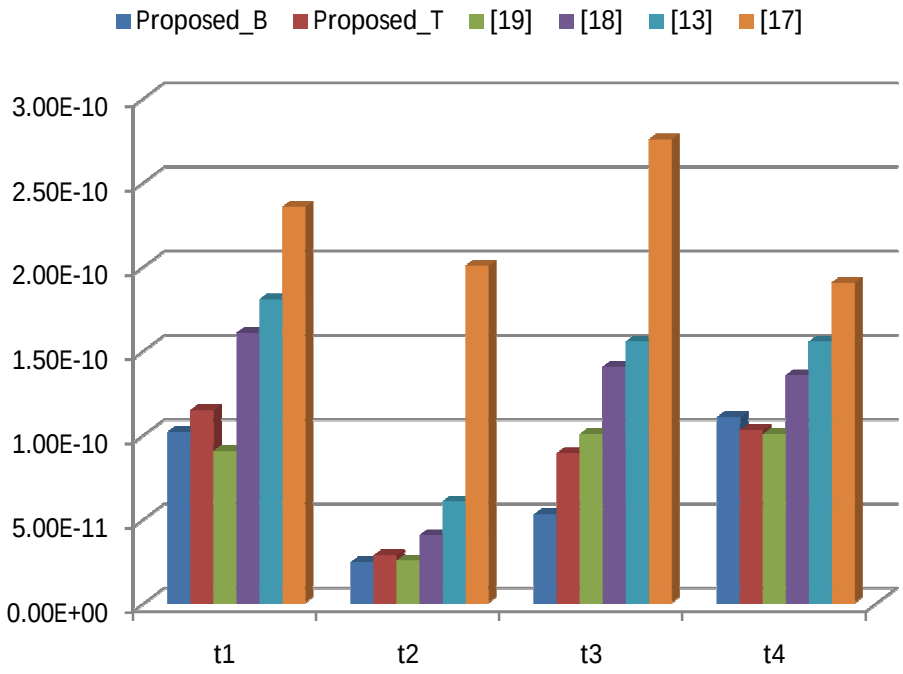


Figure 5.10: Transient response of the MIFGMOS THA using both, ternary logic gates (indicated by *Proposed_T*) and binary logic gates (indicated by *Proposed_B*) compared with other reported THA

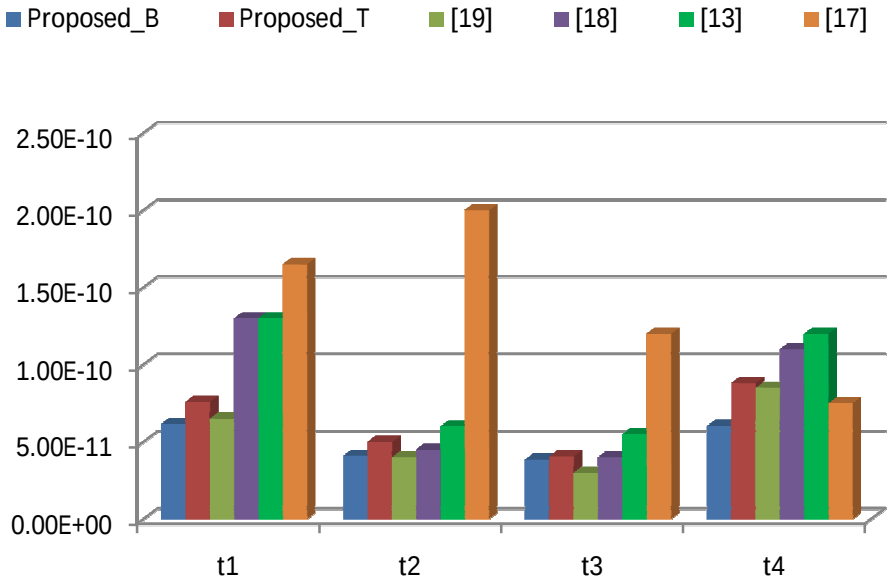


Figure 5.11: The transient delay of proposed TM circuit using both, ternary logic gates (indicated by *Proposed_T*) and binary logic gates (indicated by *Proposed_B*) compared with other reported TM

Table 5.5:Transient analysis of the designed MIFGMOS transistor for TC and THS

Ternary Combinational Circuits	**t1**	**t2**	**t3**	**t4**
Ternary Half Subtractor	137 pS	146 pS	64.9 pS	100 pS
Ternary Comparator	81 pS	56 pS	53 pS	26 pS

This research further identifies a functionality issue in the reported design of TFA and proposes a solution to the identified problem. TFS using two THS and various other ternary combinational circuits are designed and simulated using the designed ternary and binary gates, modified ternary decoder and novel TLS. An extensive simulation of the designed TALU is carried out for nine operations using TSPICE circuit simulator.

The designed novel MIFG based TALU demonstrates expected functionality and additionally signify good improvement in the performance parameters. The advantages of the designed hybrid MIFGMOS transistor based are apparent from table 5.6 and that presents a comparison of the MIFH based approach with the CNTFET [1] and QDGFET [13] based approaches reported in the literature. The circuit element count for the novel approach presented in this research combines the virtues of both the devices and specifically takes advantage of tunability and controllability of MIFGMOS transistor to facilitate the significant reduction in the circuit element count of the ternary combinational circuits as compared to earlier reported methods. It must be emphasized that the use of MIFGMOS based binary gates in the ternary combinational circuits has achieved further reduction in the circuit element count, ensuring the improvement in the timing analysis.

Table 5.6: Comparison of the circuit elements used by the MIFG based approach with other reported approaches in realization of the ternary combinational circuits

Sr. No.	Designed Ternary Circuits	Sheng *et al.* [1]	Supriya *et al.* [13]	Hybrid (MIFG-MOSFET) Approach	
				MIFG-based Ternary Gates	MIFG-based Binary Gates
1.	Ternary Decoder	20	13	**09**	**08**
2.	TLS	**--**	**--**	**04**	--
3.	THA	296	138	**108**	**91**
4.	THS	--	--	**221**	**186**
5.	1-trit TC	280	131	**93**	**76**
6.	1-trit Ternary Multiplier	168	82	**66**	**56**
7.	3: 1 Ternary Multiplexer	--	--	**25**	**--**

The simulation results of the transient timing exhibit an improvement in the performance parameters. The reduction in the number of the gates due to use of MIFGMOS transistor obviously lead to improvement in the delay. The transient response of the designed ternary combinational circuits demonstrate its functionality for various loads (1pF to 10 pF) and at various operating frequencies (500 KHz to 5 MHz). Acceptable voltage levels were obtained at the output for all these variations. This signifies good fan-out values of thedesigned ternary gates, which is an apparent advantage of operating MIFGMOS transistors at 5 V.

Another important point to be noted is the use of resistors in the designed ternary circuits. As the model parameters for MIFGMOS transistor are not available, hence standard MOS models are used to

simulate these structures. The electrical components are added to the standard MOS models to emulate the MIFGMOS transistor behavior. The equivalent circuit of MIFGMOS transistorcontains various capacitors. When this circuit is simulated using TSPICE, the problem of floating nodes arises, as a result the simulations fail to converge. As TSPICE cannot accept floating nodes having no dc path to ground, resistors are used to bypass each capacitor with a resistor. The role of these resistors is restricted only to simulation and is not considered in the layout of the circuits. The on-chip area is therefore not compromised.

The modified decoder, novel TLS and the performance analysis of the designed ternary combinational circuits validates the intelligent choice of using MIFGMOS transistor for the implementation of the TALU and thus makes the design efficient.

5.2.2 Analysis of MIFG Based Ternary Sequential Circuit

The MIFGMOS based hybrid approach for designing of combinational circuits is further extended to realize ternary sequential circuits. Ternary D flip-flop and a 2-trit synchronous counter is implemented and the functionality is verified. The implemented circuits achieve reduction in the number of MOSFETs used. The designed ternary sequential circuits are analyzed to calculate the delay and the maximum operating frequency.

5.3 The Simulation and Synthesis Results of Various Ternary Circuits

The CMOS and MIFG based implementation represent device level approach. It is necessary to further extend this to incorporate

additional inputs and functionality from the perspective of the ternary processor. The designed ternary combinational and sequential circuits are therefore further extended to VHDL implementation.

The ternary circuits as discussed in chapter 4 are synthesized using Xilinx Synthesis Tool (XST) which supports CPLD and FPGA devices. The FPGA devices that are available are only compatible to binary logic and not to ternary logic. It is however necessary to obtain synthesis summary of VHDL implementation of ternary circuits. The Spartan3E FPGA device is thus chosen to synthesis the designed ternary circuits. The Table 5.7 shows the logic in-terms of number of slices and the LUTs utilized by various ternary circuits in the Spartan3E FPGA device. As expected, the synthesis report shows the use of additional IOBs to represent the ternary logic. Total number of IOBs utilized in THA are 4 (2 inputs and 2 outputs) however the table indicates the utilization of 8 IOBs. Figure 5.12, the RTL schematic of a THA, clearly represents 8 IOBs (A-0_IBUF, A-1_IBUF, B-0_IBUF, B-1_IBUF, sum-0_OBUF, sum-1_OBUF, carry-0_OBUF, carry-1_OBUF) and use of three LUTs. Similarly the number of IOBs required by TFA, THS, TFS and TM are also exactly double the total number of inputs and outputs.

Table 5.7: Logic utilization of the ternary combinational circuits

Logic Utilization	**THA**	**TFA**	**THS**	**TFS**	**TM**	**4-trit TFA**	**4-trit TFS**
Number of Slices	2	4	2	4	2	18	18
Number of 4 input LUTs	3	8	3	8	3	32	32
Number of bonded IOBs	8	10	8	10	8	28	28

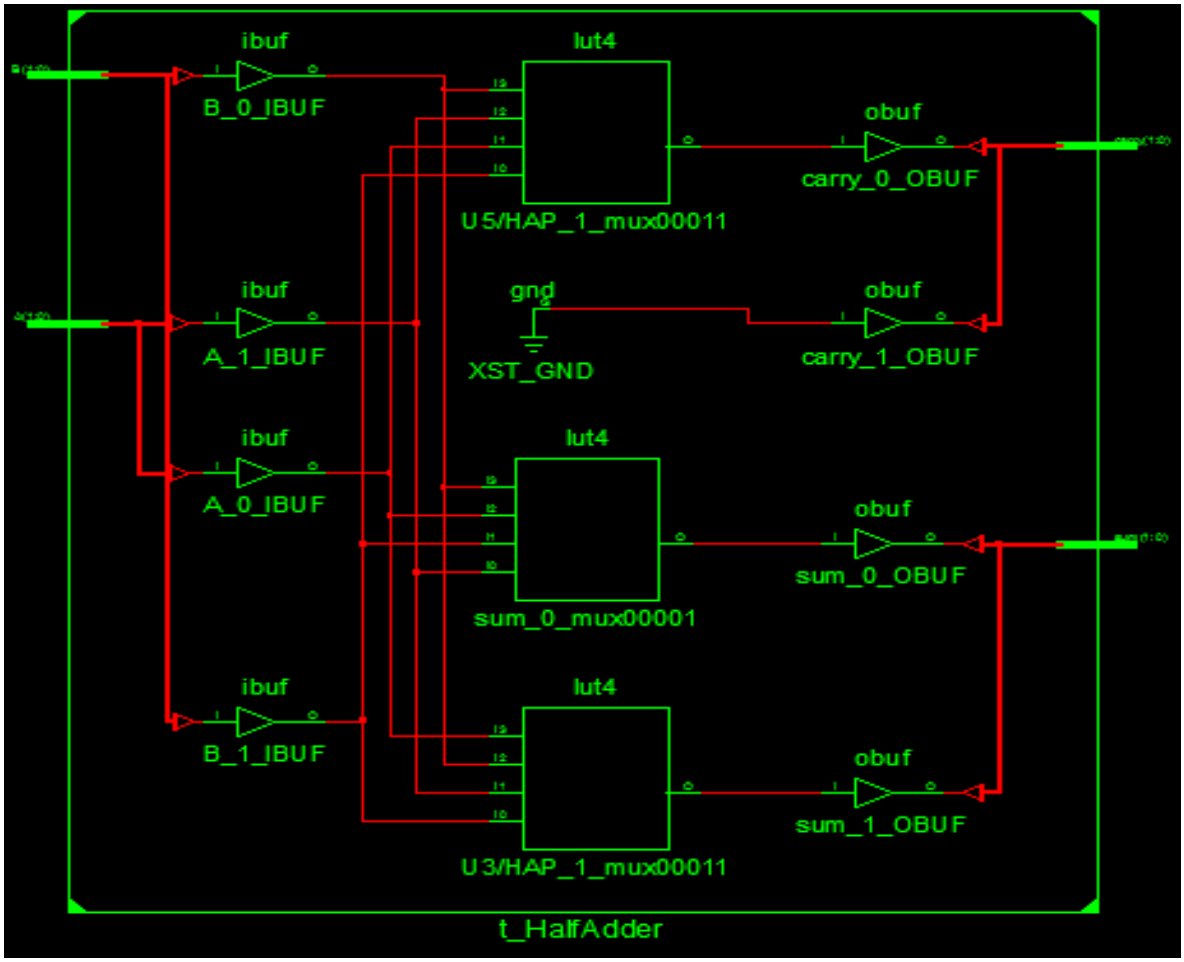


Figure 5.12: The RTL schematic of a THA

Table 5.8: Timing parameters of the ternary circuits

Timing Parameter	**1-trit THA**	**1-trit TFA**	**1-trit THS**	**1-trit TFS**	**1-trit T-M**	**4-trit TFA**	**4-trit TFS**
Data Path	B to carry	A to carry	A to Borrow	A to Borrow	A to Carry	A(0) to carry	A(0) to Borrow
Logic Delay	4.887ns	6.389ns	4.887ns	6.389ns	4.887ns	10.895ns	10.895ns
Route Delay	0.960ns	1.938ns	0.960ns	1.977ns	0.960ns	4.729ns	5.134ns
Combinational Delay	5.847ns	8.327ns	5.847ns	8.366ns	5.847ns	15.624ns	16.029ns

The table 5.8 summarizes the timing parameters of the VHDL implementation of the ternary circuits as obtained from the synthesis report. The data path from input to the carry in ternary adder and from input to the borrow output in ternary subtractor are identified as the critical data paths. The complexity in of the circuit decides the logic delay. The number of LUTs has increased substantially from 3in 1-trit THA to 8 in 1-trit TFA (as indicate din table 5.7), thus obviously leading to increase in the logic delay. The route delay has increased from 16 % to 23 %. Similarly the route delay has further increased to 32 % in 4-trit TFA. The route delay and the logic delay together contribute to the combinational delay. The combinational delay is amongst the important considerations in deciding the overall operating frequency of the ternary processor. Even though, obtained synthesis reports are merely indicative, it provides a fair idea about designing the ternary processor. The specified combinational delay must be considered when designing the TALU and the control unit of the processor. These findings further call upon the necessity of optimization techniques to improve the timing performance.

5.4 Major Contributions Of This Research

The research methodology adopted in the investigation of the ternary processor of this research can be broadly categorized in two parts:

- Switching devices for the realization of various ternary circuits
- Simulation and testing of the fundamentals units of a ternary processor

The research contributions are detailed as follows.

5.4.1 SwitchingDevices For The Realization Of VariousTernary Circuits

Voltage Injection methodisused to design the CMOS-basedternary NAND, NOR and Invertergates. The limitations of thisapproachisovercomedusing MIFGMOS transistors, that have gainedwidepopularity and are an attractive candidate for MVL. MIFGMOS transistor basedbinarygates are designed and simulated. Whendesigning the MIFGMOS transistor basedternarygates, a hybridapproachcomprising of MIFGMOS transistor and conventional MOSFET isused in the design process. The designednovelhybridapproach combines the virtues of both the deviceswhichfacilitate the significantreduction in the circuit element count of the ternarygates as compared to the earlierreportedmethods

Designing a TLS has received less attention by the researchers. This research presents a novel TLS based on MIFGMOS. The devised novel TLS exploits the controllability and tunability of the MIFGMOS transistor to achieve an intermediate voltage level and the desired functionality of the level shifter. Moreover the need of passive components and an additional power supply ($V_{DD}/2$) is completely eliminated leading to considerable reduction in the power.

The MIFGMOS based 3-trit TALU is designed using only ternary gates and combination of both, binary and ternary gates and have same architecture except the types of gates. The designed TALU has various combinational circuits namely, Ternary Half Adder (THA), TFA, Ternary Half subtractor (THS), Ternary Full subtractor (TFS), Ternary comparator, Ternary Multiplier and Ternary Multiplexer are realized using MIFGMOS transistor based approach. This research also

identifies a functionality issue in the reported design of TFA and a solution to the identified problem is presented. Literature reports design of TFA by cascading two THAs. A careful debugging of the circuit in [13], however, reveals a functionality issue in the design of full adder when A= B = C_{in} ='2'. When the input combination is *A = B = C_{in} ='2'*, it demands the C_{out} to be at logic state '2'. The term $A^2B^2C^2$ is not considered in the reported design of TFA and thus suffers from a functionality issue. This research provides a modified design of TFA that requires 36 ternary gates for the realization of TFA. A further reduction in the circuit element count of the MIFGMOS based ternary combinational circuits is achieved by replacing some of the ternary logic gates with binary logic gates. The designed MIFGMOS based approach achieves significant reduction in circuit element count and showcases improved performance parameters.

The MIFGMOS based hybrid approach for designing of combinational circuits is further extended to realize ternary sequential circuits. A D Flip-Flap-Flop is designed and its functionality is verified. Further, a ternary counter is realized which uses the D flip-flap-flop and the existing binary clock. An intelligently designed combinational circuit for the generation of the ternary states in a ternary counter ensures the reduction in the circuit element count.

Moreover, as MIFG-MOSFET is based on the already existing silicon CMOS technology, the cost of development and fabrication of MIFG-MOSFET based circuits is significantly less than that of other technologies like Carbon Nanotube FETs (CNTFETs). This also allows the use of MIFG-MOSFET in conjunction with conventional CMOS to improve the performance wherever possible and address the issues and the challenges reported in the literature

5.4.2 Simulation and Testing of the Fundamental Units of a Ternary Processor

This research presents design and implementation of an efficient TALU and TCU for a ternary processor using simulation tool and hardwired approach. The implementation of sub-program overloading feature in the designed TALU makes its design unique, flexible and portable for further extension. The designed 4 – trit TALU performs a variety of arithmetic and logical operations. The timing performance of the designed TALU, the use of special function (program status word, stack pointer, interrupt) and general purpose registers, the smooth execution of instructions with control signals signify encouraging results.

A hardwired TCU is also designed and simulated. The functionality of the TCU is verified using 65 instructions belonging to various addressing modes. The control signals required for the execution of the instructions are identified and further modeled. The implementation of sub-program overloading feature in the designed TALU makes its design unique, flexible and portable that signifies encouraging results that will pave the path for further developments in ternary processor.

Chapter 6

CONCLUSION AND FUTURE SCOPE

This chapter presents the conclusions drawn in this research and details the future scope to augment this research.

6.1 Conclusion

Despite the potential advantages of ternary logic over the binary, realization of an efficient, realistic and a practical ternary processor is still a thrust area of research.The focus of this research revolves around simulation and testing of the basic modules of ternary processor and exploring a switching device that supports ternary logic system.

MIFGMOS transistor based binary gates are designed and realized to achieve 50% reduction in the circuit elements. A novel hybrid approach based on MIFG-MOS technology for the realization of the ternary gates is designed in this research. An extensive simulation of all the designed gates is carried out using TSPICE circuit simulator. The results demonstrate expected functionality of the designed hybrid gates and additionally signify improvement in the performance parameters with reduced circuit element count.

A modified design of ternary decoder and novel TLS that has received meager attention in the reported literature is also designed in this research. It exploits the controllability and tunability of the MIFGMOS transistor to achieve an intermediate voltage level and thereby the desired functionality of the level shifter. The need of

passive components and an additional power supply is completely eliminated leading to considerable reduction in the power.

A TALU using an efficient hybrid approach based on combination of MIFGMOS transistor and conventional MOSFET is realized. This research further identifies a functionality issue in the reported design of TFA and put forward a solution to the identified problem.

The MIFG based approach is further extended to realize ternary sequential circuits. A novel and an efficient combinational circuit that generates the next state for a ternary counter, is presented in this research. The designed combinational circuit for the 2-trit ternary counter achieves significant reduction in terms circuit elements.

This research has also developed an efficient method for defining, analyzing, testing and implementing vectored TALU. Altogether 18 operations are implemented in the TALU developed from the perspective of ternary processor. The implementation of subprogram overloading feature in the TALU makes its design unique, flexible and portable for further extension. The designed control unit is simulated using an instruction set of 65 instructions to ensure that the TCU is functional and operated as expected.

The simulation results, transient analysis and comparison tables confirms the authenticity of the devised novel hybrid MIFGMOS transistor based method as well as its superiority, specifically in terms of the circuit element count and performance parameters in comparison with the other state-of-the-art ternary circuits. The designed TCU and MIFGMOS based modified decoder, novel TLS and the TALU with improvements in TFA collectively addresses few challenges, reported in the literature.

6.2 Future Directions

There remains outsized scope to further improvise the ternary processor, developed in this research. Some of the directions include

- Device level modeling using VHDLAMS (Analog Mix Signal). This will enable switch level simulation which can be used for in-depth analysis of the devised approach from the perspective of a ternary processor.
- Building standard cell library using layout tools for ternary circuits will further speed up the design and layout process. For any processor this will be a complex process. Readily available standard cell library will simplify the task.
- Developing a synthesis tool that supports ternary logic. The existing FPGA and CPLD are compatible with binary logic. Availability of synthesis tool supporting ternary logic will provide detail information for the hardwire realization.
- Pipeline execution of the instructions and designing instructions with fixed machine cycles will improve the execution speed and help to improvise the specifications of the processor.
- With the availability of standard libraries, synthesis tools, VHDLAMS and ternary memories will enable implementation and realization of MIFGMOS based fully functional ternary processor.
- Explore the other potential beyond CMOS technologies like FINFET and HEMT from ternary perspective and hybrid approaches for realization of ternary gates.

RESEARCH PUBLICATIONS

The following research papers are published and communicated:

Paper under review

1. Narkhede S. S., Chaudhari B. S., Kharate G. K., "An Efficient MIFGMOS Transistor Based Design of Ternary ALU Using Novel Ternary Level Shifter" Journal of Information Processing System, Computer Systems and Theory, South Korea, submitted in June 2015.

Papers Published in International Journals

1. Narkhede S. S., Chaudhari B. S., Kharate G. K,"A Novel Hybrid MIFG-CMOS Based Approach For The Realization of Ternary Gates" ICTACT Journal on Microelectronics, vol.1 (2), 2015, pp. 45-56.

2. Narkhede S. S., Chaudhari B. S., Kharate G. K, "Design and Implementation of Efficient Ternary Control Unit". Journal of VLSI Design Tools and Technology (Scientific Technical Medical, STM Journal), vol. 5 (3), 2015, pp. 55-70.

3. Narkhede S. S., Chaudhari B. S.,Kharate G. K, "Design and Implementation of an Efficient Instruction Set for Ternary Processor" International Journal of Computer Application, vol. 83(16), 2013, pp. 33-39.

4. Narkhede S. S., Chaudhari B. S., Kharate G. K, "A VHDL Implementation of Ternary Arithmetic and Logic Unit for Multi Valued Processor" CIIT PDCS, vol. 7, no. 6, 2015 pp.185-193.

Papers Published in International Conference:

1. Dhande A. P., Narkhede S. S., Dudam S. S., VLSI Implementation Of Ternary Gates Using Tanner Tool" 2nd IEEE International Conference on Devices, Circuits and Systems (ICDCS), 2014, Coimbatore, pp. 1-5.

REFERENCES

[1] Sheng, L., Yong-Bin, K., Fabrizio, L. 'CNTFET- based design of ternary logic gates and arithmetic circuits', IEEE transactions on nanotechnology, 10(2), March 2011.

[2] M. A. H. Abdul karim "A ternary J-K memory", Proc. IEEE ISMVL pp. 221-225, May 1976.

[3] R. E. Miller "Switching theory, John Wiley, 1965"

[4] Masahiro, S., Mititada, M., 'A study of ternary fuzzy processor using neural networks' ISCAS'97., Proceedings of 1997 IEEE International Symposium on circuits and systems,1, pp. 613-616,1997

[5] K. C. Smith, "The prospects for multivalued logic: A technology and application view," IEEE Trans Comput, vol. C-30, pp. 619-634, Sept. 1981.

[6] Moaiyeri, Mohammad H., Reza F. M., Akbar D., Keivan N, and Omid H. "A Universal Method for Designing Low-Power Carbon Nanotube FET-Based Multiple-Valued Logic Circuits." IET Computers & Digital Techniques 7, no. 4, pp. 167-181, 2013.

[7] Epstein, George, Gideon Frieder, and David C. Rine. "The development of multiple-valued logic as related to computer science." Computer 9 (1974): 20-32.

[8] Vudadha C, Katragadda S., Phaneendra P. "2:1 multiplexer-based design for ternary logic circuits" 2013IEEE Asia pacific Conference on Postgraduate research in Microelectronics and Electronics, Dec 2013, pp. 46-51

[9] Bala P C, A. Antoniou , "Low Power dissipation MOs ternary logic family", IEEE Journal of Solid State Circuits, vol. sc-19, no 5, pp. 739-749, 1984.

[10] Rozon, C.: 'On the use of VHDL as a multi-valued logic simulator'. Multiple-Valued Logic, 1996. Proceedings of 26th International Symposium on. IEEE, 1996, pp 110-115.

[11] Dhande, A., Ingole, T.: 'Design and implementation of 2 bit ternary ALU slice' 3rd International conferences sciences of electronics, technologies of information and telecommunication, March 2005, Tunsia pp. 1- 11.

[12] Dhande, A., Jaiswal, R., Dudam, S.: 'Ternary Simulator Using VHDL', 4th International conference sciences of electronic technologies of Information and Telecommunications, March 2007, Tunsia. pp 1-7.

[13] Supriya K., John C., Jain F. C., "Design of Ternary Logic Combinational circuits Based on Quantum Dot Gate FETs", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, volume:21 , Issue: 5, pp.793-806, 2013.

[14] Plummer J., Griffan P B, "Material and Process limits in silicon VLSI technology, "Proceedings of IEEE, vol. 89, issue 3, pp. 242-258, 2001

[15] Ragini, K., M. Satyam, and B. C. Jinaga. "Variable Threshold MOS Circuits."International Journal of Modern Engineering Research (IJMER) Vol. 3, Issue. 6, Nov - Dec. 2013 pp-3632-3640

[16] Serran N, Martins J, Dias J, 'A proposal for the implementation of ternary digital circuits', microelectronics Journal 28, 1997, pp. 533-541.

[17] Rizwan, B.: 'Current mode signaling in deep sub-micrometer global interconnects', IEEE transactions on very large scale integration (VLSI) systems, 11(3), 2003, pp. 406-417.

[18] Raychowdhury, A., Kaushik, R.: 'A novel multiple valued logic design using ballistic carbon nanotube FETs' , Proceedings of the 34th IEEE international symposium on multiple valued logic (ISMVL '04), pp 14-19.

[19] J. Lukasiewicz. O logicetr`ojwarto`sciowej (tr. on three-valued logic). RuchFilozoficzny, vol. 5, pp. 169–171, 1920.

[20] Miller, D. Michael, and Mitchell A. Thornton. "Multiple valued logic: concepts and representations." *Synthesis lectures on digital circuits and systems* 2, no. 1 (2007): 1-127.

[21] E. L. Post. Introduction to a general theory of elementary propositions. Amer. J. Math., vol. 43, pp. 163–185, 1921, doi:10.2307/2370324

[22] S. C. Kleene. On a notation for ordinal numbers. The Journal of Symbolic Logic, vol. 3, pp. 150–155, 1938, doi:10.2307/2267778.

[23] Milton R., Martins, E., Richardi, S. 'Multiple valued logic Algebra for the synthesis of digital circuits' 39th international symposium on multi-valued logic , ISMVL, 2009, May 2009, pp 262-267

[24] Dr Esther Rodriguez-Villegas, *Low Power and Low Voltage Circuit Design with the FGMOS Transistor,* The Institution of Engineering and Technology, 2006.

[25] Hagen, Øyvind. "Multiple-Input Common-Gate FGUVMOS Transistor and Its Application in Multiple-Valued Logic Circuits." (2006).

[26] Ester R. V., "Low Power and Low Voltage Circuit Design with the FGMOS Transistor", IET Circuits, Devices and systems series 20, published by the Institution of Engineers and Technology, 2006.

[27] Topór-Kamiński, L., and P. Holajn. "Multiple-input floating-gate MOS transistor in analogue electronics circuit." *TECHNICAL SCIENCES* 52, no. 3 (2004).

[28] Halpern, Israel, and Michael Yoeli. "Ternary arithmetic unit." In *Proceedings of the Institution of Electrical Engineers*, vol. 115, no. 10, pp. 1385-1388. IET Digital Library, 1968.

[29] Wang et al, "Low power dynamic ternary logic", IEEE proceedings –circuits, devices and systems, vol. 135, issue: 6, pp: 221-230, December 1988.

[30] Mukaidono, Masao. "Regular Ternary Logic Functions? Ternary Logic Functions Suitable for Treating Ambiguity." *IEEE transactions on computers* 2 (1986): 179-183.

[31] Hu, Mou, and Kenneth C. Smith. "Ternary scan design for VLSI testability." *Computers, IEEE Transactions on* 100, no. 2 (1986): 167-170.

[32] Seger, C-J., and Janusz A. Brzozowski. "An optimistic ternary simulation of gate races." *Theoretical computer science* 61, no. 1 (1988): 49-66.

[33] Morisue, M., and K. Suzuki. "A Josephson ternary associative memory cell." *Magnetics, IEEE Transactions on* 25, no. 2 (1989): 849-852.

[34] Morisue, M., K. Oochi, and M. Nishizawa. "A novel ternary logic circuit using Josephson junction." *Magnetics, IEEE Transactions on* 25, no. 2 (1989): 845-848.

[35] Rizvi, Aftab A., K. Zaheer, and M. S. Zubairy. "Design of ternary half-adder and-subtractor using frequency modulation in grating structures." *Optics communications* 84, no. 5 (1991): 247-250.

[36] Jones, Trevor H., and Il-Yeol Song. "Analysis of binary/ternary cardinality combinations in entity-relationship modeling." *Data & Knowledge Engineering* 19, no. 1 (1996): 39-64.

[37] Serran, N. V., and J. Dias. "A proposal for the implementation of ternary digital circuits." In *Microelectronics, 1995. Proceedings., 1997 20th International Conference on*, vol. 2, pp. 485-490. IEEE, 1997

[38] Srivasta, A. "Back Gate Bias Method of Threshold Voltage Control for the design of Low Voltage CMOS Ternary Logic Circuits" Microelctron. Reliab. Elsevier, vol. 40, (12), pp 2107-2110, 2000.

[39] Nascimento L.: 'An automated tool for analysis and design of MVL digital circuits', 14th IEEESymposium on Integrated Circuits and Systems Design, 2001,pp. 52-57

[40] Yamamoto Y. "An extension of ternary majority function and its application to evlvable system" Proceedings of 33rd International Symposium on Multiple-valued logic, 2003, pp. 17-23

[41] Maddess, T., Y. Nagai, A. C. James, and A. Ankiewcz. "Binary and ternary textures containing higher-order spatial correlations." *Vision research* 44, no. 11 (2004): 1093-1113.

[42] Gundersen, Henning, and Yngvar Berg. "A novel ternary switching element using CMOS recharge semi floating-gate devices." In *null*, pp. 54-58. IEEE, 2005.

[43] Ali, H., Hamdam, M., Rashid, M., Hamied, H., Issa, A., Kassem, A.: 'A novel neural network ternary arithmetic logic unit', The 23rd international technical conference on circuits / systems, computers and communications (ITC-CSCC 2008), pp. 593-596.

[44] Sadik et al, "Towards a Ternary Sigma Delta Modulated Processor", IEEE 8th International Conference on Computer and Information Technology Workshops, vol. 8, pp: 515 – 520, July 2008.

[45] Satishkumar A, Priya A, "Minimization of Ternary Combinational Circuits – A Survey" , International journal of engineering science and Technology, vol. 2(8), 2010, 3576-3589, pp: 3576-3589

[46] Lang, Yan-Feng, Ji-ZhongShen, Liang Geng, and Mao-Qun Yao. "Design of ternary clock generator." *Electronics Letters* 50, no. 15 (2014): 1052-1054.

[47] Anand A, Sushanta M, Anindita D and B. Shivalal, "FGMOS Based Low-Voltage Low-Power High Output Impedance Regulated Cascode Current Mirror." International Journal of VLSI Design & Communication Systems (VLSICS) vol. 4, pp. 39-50., 2013

[48] Cruz A, and L. Noe, "Mismatch Compensation in Current Mirrors with FGMOS Transistor." In Electrical Engineering Computing Science and Automatic Control (CCE), 7th International Conference on, pp. 599-603. 2010

[49] H. T. Mouftah, K. C. Smith, 'Injected voltage low power CMOS for 3 valued logic' IEE Proceeding, vol 129, Pt G, No. 6, Dec 1982.

[50] Dhande, A. P., Satish S. Narkhede, and Shridhar S. Dudam. "VLSI implementation of ternary gates using Tanner Tool." In *Devices, Circuits and Systems (ICDCS), 2014 2nd International Conference on*, pp. 1-5. IEEE, 2014.

[51] Perry, Douglas. VHDL: programming by example. Tata McGraw-Hill Education, 2002.

[52] Rashmi, D., Pravin, D., Sonali, D.: 'TFET based ternary logic gates and arithmetic circuits', National conference on innovative paradigms in engineering and technology, (pub. Int. journal of computer applications)

[53] Irving, Thurman, Sajjan G. Shiva, and H. Troy Nagle Jr. "Flip-flops for multiple-valued logic." *Computers, IEEE Transactions on* 100, no. 3 (1976): 237-246.

[54] Mouftah, H. T., and I. B. Jordan. "Design of ternary COS/MOS memory and sequential circuits." *Computers, IEEE Transactions on* 100, no. 3 (1977): 281-288.

[55] SAMUEL TUAN WANG "On the */-V* Characteristics of Floating-Gate MOS Transistors" IEEE *transactions on electron devices*, vol. Ed-26, no. 9, September 1979

[56] Serra, M. "Applications of Multi Valued Logic to Testing of Binary and MVL Circuits" , International Journal Electron, vol. 63, issue: 2, pp: 197-214, 1987

[57] Wu, X. W., and F. P. Prosser. "CMOS ternary logic circuits." *IEE Proceedings G (Circuits, Devices and Systems)* 137, no. 1 (1990): 21-27.

[58] Chung et al, "A new two phase pipelined dynamic CMOS ternary logic", IEEE international symposium on circuits and systems, vol. 1, pp: 582 – 586, May 1990.

[59] Rajashekhara, T., and I-Shi Chen. "A fast adder design using signed-digit numbers and ternary logic." In *Southern Tier Technical Conference, 1990., Proceedings of the 1990 IEEE*, pp. 187-194. IEEE, 1990.

[60] Wu X, and Prosser F. "Cmos Ternary Logic Circuits." IEE Proceedings on Circuits, Devices And Systems, 137.1, pp. 21-27, 1990.

[61] Frederic Mailhot, Ph.D thesis 'Technology mapping for VLSI circuits exploiting Boolean properties and operations', Dec 1991.

[62] Butler, Jon T. *Multiple-valued logic in VLSI design*. IEEE Computer Society, 1991.

[63] Tadashi Shibata, TadahiroOhmi, "A Functional MOS transistor featuring gate level weighted sum and threshold operations" *IEEE Trans. Electron Devices,* vol.39, no.6,pp.1444-1455, June 1992

[64] Wang, Samuel Tuan. "On the IV characteristics of floating-gate MOS transistors." IEEE Transactions on Electron Devices 26, pp. 1292-1294, 1992

[65] T. Shibata and T. Ohmi, *Neuron MOS. binary- logic integrated circuits-PartII: "Simplifying techniques of circuit configuration and their practical applications*, IEEE Trans. on Electron devices, vol. 40, no. 5, pp. 974-979, May 1993.

[66] Chung et al, "Design and application of pipelined dynamic CMOS Ternary logic and simple ternary differential Logic", IEEE journal of solid state circuits, vol. 28, no. 8, pp: 895 – 906, August 1993.

[67] T. Shibata and T. Ohmi, "*Neuron MOS. binary-logic integrated circuits-Part I: Design fundamentals and soft-hardware logic circuit implementation*", IEEE. Trans. on Electron devices, vol. 40, no. 3, pp. 570-575, March 1993.

[68] Forster A, "Resonant Tunnelling Diodes: The Effect Of Structural Properties on Their Performance" Advances In Solid State Physics, vol : 33, NewYork, Springer –Verlag, pp. 37-62, 1994.

[69] C. -J. H. Seger and R. E. Bryant. Formal verification by symbolic evaluation of partially ordered trajectories. Formal Methods Syst. Design: An Int. J., vol. 6, pp. 147–189, 1995,doi:10.1007/BF01383966

[70] Hamacher, V. Carl, Zvonko G. Vranesic, Safwat G. Zaky, Zvonko Vransic, and Safwat Zakay ,'Computer organization. Edition 5, McGraw-Hill, 1996, chapter 7.

[71] Morisue et al, "A novel Josephson ternary multiplier", IEEE transactions on applied superconductivity, vol. 7, no. 2, pp: 2979-2982, June 1997.

[72] Daniel Foty,*MOSFET modeling with SPICE*, Prentice Hall, 1997.

[73] Segura, J., J. L. Rossello, J. Morra, and H. Sigg. "A variable threshold voltage inverter for CMOS programmable logic circuits." *IEEE Journal of Solid-State Circuits* 33, no. 8 (1998): 1262-1265.

[74] Elena Dubrova, 'Multi-Valued Logic in VLSI: Challenges and Opportunities' Proceedings of NORCHIP, vol. 99, pp. 340-350. 1999.

[75] Iwai, H.: 'CMOS Technology – year 2010 and beyond', IEEE Journal of Solid State Circuits, SC -34, 3, 1999, pp. 357-366.

[76] Stephen, H.: 'High speed digital system design', John Wiley and Sons, Inc. 2000, pp. 74-90.

[77] Shen, Jing, Motoi Inaba, Koichi Tanno, and Okihiko Ishizuka. "Multi-valued logic pass gate network using neuron-MOS transistors." In Multiple-Valued Logic, 2000.(ISMVL 2000) Proceedings. 30th IEEE International Symposium on, pp. 15-20. IEEE, 2000.

[78] Nascimento L.: 'An automated tool for analysis and design of MVL digital circuits', 14th IEEESymposium on Integrated Circuits and Systems Design, 2001,pp. 52-57

[79] A. Srivastava and C. Srinivasan "ALU DESIGN USING RECONFIGURABLE CMOS LOGIC," Proc. IEEE International Conference on Electron Devices,2002

[80] Perry, Douglas. VHDL: programming by example. Tata McGraw-Hill Education, 2002.

[81] Harish N. Venkata "Ternary and quaternary logic to binary bit conversion CMOS integrated circuit design using multiple input floating gate MOSFETS" 2002

[82] Sowmya Subramanian "Ternary logic to binary bit conversion using multiple input floating gate MOSFETS in 0.5-micron n-well CMOS technology" 2002

[83] Chandra Srinivasan" Arithmetic logic unit (ALU) design using reconfigurable CMOS logic" 2003

[84] Topor-K. and P. Holajn, "Multiple-Input Floating-Gate MOS Transistor in Analogue Electronics Circuit" Bulletin of the polish academy of sciences technical sciences, technical sciences , vol. 52 , no. 3, pp. 251-256, 2004.

[85] Alfredsson, Jon, Snorre Aunet, and Bengt Oelmann. "Basic speed and power properties of digital floating-gate circuits operating in subthreshold." In IFIP International Conference on Very Large Scale Interaction, pp. 229-232. Edith Cowan Univ, 2005.

[86] Delgado-Frias, José G., Jabulani Nyathi, and Suryanarayana B. Tatapudi. "Decoupled dynamic ternary content addressable memories." Circuits and Systems I: Regular Papers, IEEE Transactions on 52, no. 10 (2005): 2139-2147.

[87] Dhande, A. P., and V. T. Ingole. "Design of 3-Valued RS & D Flip-Flops Based on Simple Ternary Gates." International Journal of Software Engineering and Knowledge Engineering 15, no. 02 (2005): 411-417.

[88] Arjit R, "carbon-Nanotube-Based voltage Mode Multiple- Valued Logic Design" , IEEE Transactions on Nanotechnology, vol. 4 no(2), 2005, pp. 168 - 179

[89] Gundersen, Henning, and Yngvar Berg. "A balanced ternary multiplication circuit using recharged semi-floating gate devices." In Norchip Conference, 2006. 24th, pp. 205-208. IEEE, 2006.

[90] D. M Miller, M. A. Thornton, 'Multi Valued Logic: Concepts and Representations' synthesis lectures on digital circuits and systems, 2007, vol: 2, No.1 , pg 1-127.

[91] Jon A., Snorre A., and Bengt O. "Small Fan-in Floating Gate Circuits with Application to an Improved Adder Structure." 20th International Conference on VLSI designs, pp: 314-317, 2007.

[92] Mozammel, K.: 'Quantum ternary parallel adder / subtractor with partially –look-ahead carry' Journal of system architecture, 2007, 53, pp 453-464.

[93] Mozammel, K.: 'A recursive method for synthesis quantum / reversible quaternary parallel adder/ subtractor with look-ahead carry' Journal of system architecture, 54 (2008) pp. 1113-1121.

[94] Haider, A. M, AI-rifai, F, Alaeldine, A. Bernard M. F.'A novel ternary controller unit'3rd International Conference on Information and Communication Technologies: From Theory to Applications, 2008. ICTTA 2008, pp 1-6.

[95] Gorde, K., Deshmukh. P.: 'Design and Simulation of Ternary Logic Based Arithmetic Circuits', Proceedings of the 2009 International Conference on Signals, Systems and Automation (ICSSA 2009). Universal-Publishers. com, 2010

[96] Satish Kumar, A., SwetaPriya, A., 'Modeling of combinational circuits based on ternary multiplexers using VHDL', International journal of computer science and engineering, 2(5), 2010, 1777-1791.

[97] Kotiyal, S., Himanshu, T., Nagarajan, R.: 'Design of A ternary barrel shifter using multiple valued reversible logic', Proceeding of 10th IEEE international conference on nanotechnology, korea 2010, pp. 1104-1108.

[98] Jesús de la Cruz Alejo, L. NoeOliva Moreno "Mismatch Compensation in Current Mirrors with FGMOS Transistor"7th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE 2010)

[99] De La Cruz Blas, Carlos, and Michael M. Green. "Floating-gate CMOS ternary latch." Electronics letters 46, no. 18 (2010): 1260-1262.

[100] Gorde, K., Deshmukh. P.: 'Design and Simulation of Ternary Logic Based Arithmetic Circuits', Proceedings of the 2009 International Conference on Signals, Systems and Automation (ICSSA 2009). Universal-Publishers. com, 2010.

[101] Murthy, PH ST, L. Madan Mohan, V. Sreenivasa Rao, and V. Malleswara Rao. "4T Carry Look Ahead Adder Design Using MIFG." In Information and Communication Technologies, pp. 490-494. Springer Berlin Heidelberg, 2010.

[102] Sipos, E., and C. Miron. "Master-Slave ternary D flip-flap-flops with triggered edges control." In Automation Quality and Testing Robotics (AQTR), 2010 IEEE International Conference on, vol. 2, pp. 1-6. IEEE, 2010.

[103] Moaiyeri, Mohammad Hossein, Akbar Doostaregan, and KeivanNavi. "Design of energy-efficient and robust ternary circuits for nanotechnology." IET Circuits, Devices & Systems 5, no. 4 (2011): 285-296.

[104] Ullah, Zahid, Kim Ilgon, and SanghyeonBaeg. "Hybrid partitioned SRAM-based ternary content addressable memory." Circuits and Systems I: Regular Papers, IEEE Transactions on 59, no. 12 (2012): 2969-2979.

[105] Lin, Sheng, Yong-Bin Kim, and Fabrizio Lombardi. "Design of a ternary memory cell using CNTFETs." Nanotechnology, IEEE Transactions On 11, no. 5 (2012): 1019-1025.

[106] Multi-Valued Logic Applications in the Design of Switching Circuits

[107] Zhou, Xuanchang, and Guoqiang Hang. "Design of ternary D flip-flop using one latch with neuron-MOS literal circuit." In Natural Computation (ICNC), 2013 Ninth International Conference on, pp. 272-276. IEEE, 2013.

[108] Joshi, Samir B., J. C. Prajapati, and B. H. Soni. "Analysis and Study of FGMOS Based Current Mirror Circuit Using 0.35 μm Technology." International Journal of Engineering and Innovative Technology (IJEIT), Volume 2, Issue 10, April 2013

[109] Chandurkar, Miss Ankita P., Miss Mamta Sarde, and Miss Priyanka S. Vyawahare. "Design Of Ternary Arithmetic Circuits." IORD Journal of Science & Technology E-ISSN: 2348-0831 Volume 1, Issue IV (MAY-JUNE 2014) PP 43-47

[110] Hang, Guoqiang, Xuanchang Zhou, and Xiaohui Hu. "Design of Dynamic Digital Circuits with n-Channel Multiple-Input Floating-Gate Transistors." In Dependable, Autonomic and Secure Computing (DASC), 2014 IEEE 12th International Conference on, pp. 447-452. IEEE, 2014.

[111] Hang, Guoqiang, Xiaohua Li, and Xiaohui Hu. "Design of dynamic ternary logic using floating-gate MOS transistor." In Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on, pp. 1-3. IEEE, 2014.

[112] Karmakar, Supriya. Novel Three-state Quantum Dot Gate Field Effect Transistor. Springer, 2014.

[113] Gaikwad, V. T., and P. R. Deshmukh. "Design of CMOS ternary logic family based on single supply voltage." In Pervasive Computing (ICPC), 2015 International Conference on, pp. 1-6. IEEE, 2015.

[114] Narkhede, S. S., B. S. Chaudhari, and G. K. Kharate. "a novel MIFGMOS transistor-based approach for the realization of ternary gates."ictact journal on microelectronics, july 2015, volume: 01, issue: 02

[115] Karmakar, Supriya, and Faquir C. Jain. "Ternary static random access memory using quantum dot gate field-effect transistor." Micro & Nano Letters 10, no. 11 (2015): 621-624.

[116] Jimmy, Sutaria, and Satish Narkhede. "Design of ternary D latch using carbon nanotube field effect transistors." In Electronics and Communication Systems (ICECS), 2015 2nd International Conference on, pp. 151-154. IEEE, 2015.