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PERFORMANCE ANALYSIS OF 32NM FINFET AND CNFET OSCILLATOR CIRCUIT IN SUB THRESHOLD REGIME

Shridhar S. Khule[1] and Rupali A. Walunj[2]

[1]*Department of Electrical Engineering, Savitribai Phule Pune University, India*
[2]*Department of Electronics and Telecommunication Engineering, Savitribai Phule Pune University, India*

Abstract

The proliferation of portable electronics imposes a pressing need on design of low power circuits. Sub threshold circuits are the ideal candidate for design of ultra low power circuit. However, this ultra low power consumption is achieved by MOSFET based sub threshold circuits at the cost of deteriorated performance and exacerbated variability. According to International Technology Roadmap for Semiconductors (ITRS) FinFET and CNFET are the promising alternatives to MOSFET. This paper, therefore investigates the performance of sub threshold Voltage Controlled Oscillator (VCO) designed using Double Gate-FinFET (DG FinFET) and CNFET. Five stage DG FinFET based and CNFET Current Starved Voltage Controlled Oscillator (CSVCO) is designed in HSPICE and simulation results are analyzed. The results indicate that CNFET oscillator exhibits better PDP compared to DG-FinFET CSVCO by 89.11% at 200mv supply voltage. Also, the variability analysis shows that CNFET VCO is more robust to process and temperature variations compared to DG FinFET VCO and is therefore an adequate choice for weak inversion region.

Keywords:

Current Starved VCO (CSVCO), FinFET, Carbon Nano Tube Field Effect Transistors (CNFET), Power Delay Product (PDP), Energy Delay Product (EDP), Energy Efficiency

1. INTRODUCTION

Technology scaling has resulted in revolutionary growth of semiconductor industry. However, the shrinkage of MOSFET in nanometer regime faces certain manufacturing challenges. Moreover, the adverse effect of short channel like Drain Induced Barrier Lowering (DIBL), punch through etc. leads to poor electrostatic control of gate on channel and obstructs further scaling of device. ITRS has predicted that the technology scaling will confront serious limitations in deep nanometer regime. Researchers have recommended certain solutions like changing the structure of planar MOSFET device or changing the channel material to improve the electrostatic control and thereby performance of device. DG-FinFET (a 3D structure) and CNFET technology have emerged as an alternative device for CMOS in deep nanometer regime [1].

The tremendous demand of battery operated portable electronic gadgets has diverted the focus of VLSI circuit designers from high speed to energy efficient circuits. Moreover, for certain applications like wireless sensor nodes, pace makers, RFID tags and hearing aids etc., low power circuits are preliminary requirement since, battery charging or replacement is infeasible. Transceivers are incorporated in communication sub systems in these applications. VCO is a prime block in transceivers systems and therefore design of energy efficient VCO will certainly enhance the energy efficiency of these power sensitive applications [2]. Moreover, VCO is a key block in a system that has a dominant impact on the performance and power consumption [3]. Also, VCO is most power hungry block in Phase Locked Loops (PLL) and therefore determines the power consumed by PLL [4-5].

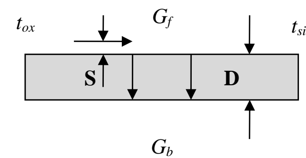
Sub threshold circuits are ideal candidates to achieve ultra low power [6]. However, MOSFET based sub threshold circuits exhibits deterioration in performance and elevated sensitivity to process and temperature variations. This paper therefore, investigates the performance of sub threshold VCO with the upcoming technologies like CNFET and FinFET.

Section 2 gives overview of DG FinFET and CNFET device followed by description of CSVCO circuit in Section 3. Section 4 explores the performance of DG FinFET and CNFET CSVCO and finally conclusion is drawn in section 5.

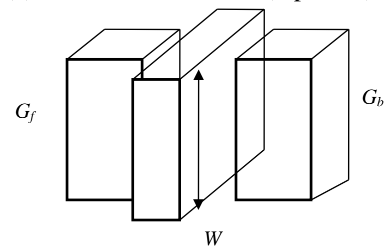
2. BACKGROUND

2.1 DOUBLE GATE FINFET

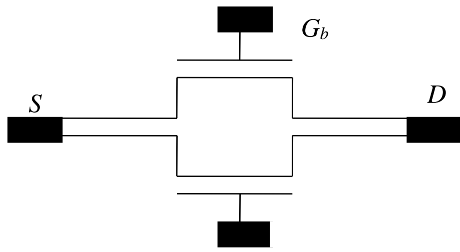
The two electrically coupled gates in Double Gate transistor technology facilitate the improvement in electrostatic control of gate over thin silicon body. Among the double gate transistor architectures, FinFET is the most attractive choice because of the self-alignments of two gates and the similarity in fabrication steps with existing MOSFET technology. In contrast with the horizontal channel in planar MOSFET, the channel in FinFET is vertical. The 3D structure of FinFET with thin silicon body wrapped by the gate improves the sub threshold swing and hence the switching frequency compared to planar MOSFET. The width of FinFET is decided by the height of channel [7]. Double gate Fin-FET improves the electrostatic control of the gate thereby increasing performance.



(a) Front and Rear Gate (top view)



(b) 3dimensional view



(c) The DG FinFET sub-circuit model

Fig.1. Conceptual model of DG FinFET [8]

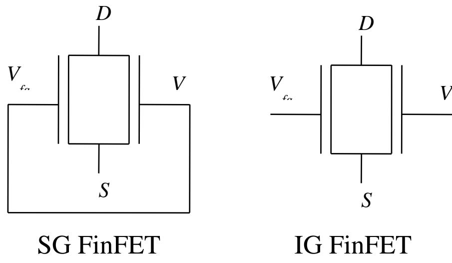


Fig.2. FinFET Configuration

The DG Fin FET structure and its model is depicted Fig.1(a)-Fig.1(c) [8]. The two configurations of DG FinFET viz. SG (three terminals) and IG (four terminals) are illustrated in Fig.2. SG configuration of DG FinFET shows better performance [9]-[12] whereas IG double gate devices exhibits improved flexibility [13]-[14].

2.2 CNFET

CNFETs are the promising candidates and better alternative to the CMOS devices in upcoming future technologies [1]. These nano transistors employs the carbon nano tube (CNT) or array of CNTs as a channel material. CNTs are the tubes obtained by rolling the grapheme sheets. The atomic structure of CNTs, referred to as chirality, decides the conductivity of the CNTs [15]-[16].

The Fig.3 illustrates the basic structure of CNFET. CNTs, the channel of device, rest on bulk and are controlled by the metal gate electrode. In this work, CNFET model developed by Stanford University is used [17]-[18]. It is a MOSFET-like CNFET that uses a top-gate structure. Figure 4 illustrates the cross sectional view and top view of MOSFET like CNFET. MOSFET-like CNTFET proves to be an appropriate choice for CMOS circuits [19]. The source and drain (un-gated portion of CNT) are heavily doped semiconducting CNTs with P_d metal contacts while the channel (gated portion of CNT) is un-doped. Eq.(1) illustrates the CNT diameter,

$$D_{CNT} = \frac{a\sqrt{m^2 + mn + n^2}}{\pi} \tag{1}$$

where m and n defines the chiral index, a (≈2.49e-10) is the constant that specify distance between the atoms, D_{CNT} represents CNT diameter

The threshold voltage of CNFET can be expressed as

$$V_{TH} = \frac{\sqrt{3}}{3}\frac{aV_{\pi}}{eD_{CNT}} \tag{2}$$

where V_{π} is 3.033ev and gives energy of the carbon π-π bond, e is a fundamental constant which express unit of electric charge.

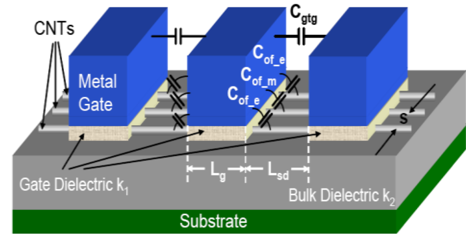
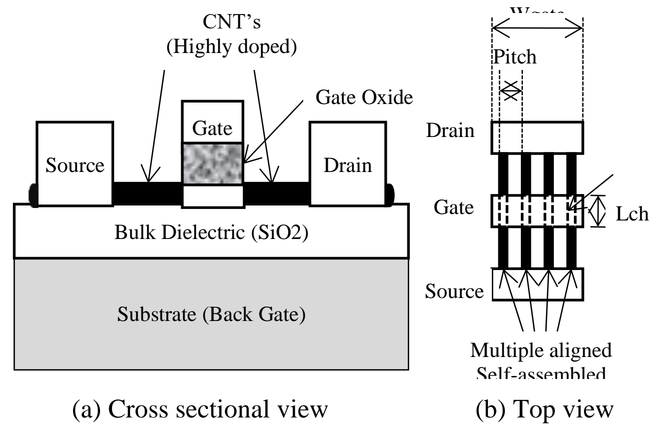


Fig.3.Basic structure of CNFET



(a) Cross sectional view (b) Top view

Fig.4. MOSFET like CNFET structure

3. CURRENT STARVED VCO

Ring oscillator is a simple close loop circuit formed from inverters. Ring oscillators consume low power, are area efficient and therefore are an attractive option for portable applications which have low power consumption as their preliminary requirement. Ring oscillator with output frequency controlled by input control voltage constitutes CSVCO.

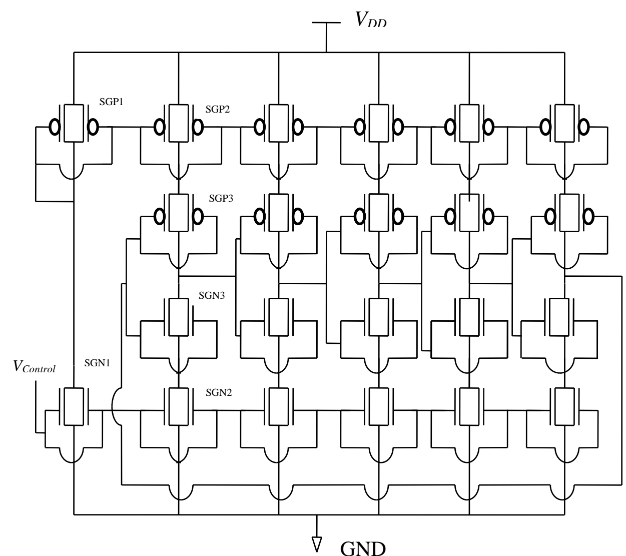


Fig.5(a). SG FinFET VCO

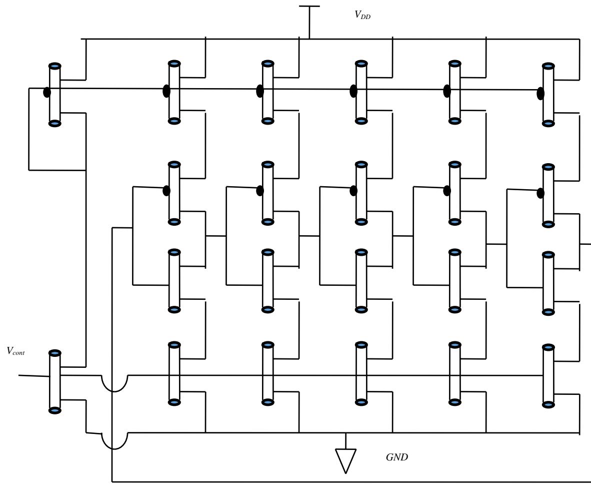


Fig.5(b). CNFET VCO

The frequency of *N* stage CSVCO is expressed as [20],

$$f_{oscillator} = \frac{I_d}{N * C_{Tot} * V_{DD}} \quad (3)$$

where I_d represents the driving current, C_{Tot} is the total capacitance and V_{DD} is the supply voltage.

SG FinFET CSVCO is depicted in Fig.5 (a). SGP3 and SGN3 form the inverter. SGP2 sources the current whereas SGN2 acts as sink. $V_{control}$, controls the drive current in SGP1 and SGN1. Since the gate and source potential of SGP1 and SGP2 is same, SGP2 carries the same current as SGP1 and sources it into the inverter. This is true for all current sources. Thus, the current set by the control voltage is reflected in each inverter stage. Therefore, the operating frequency, which is function of drive current, can be controlled by the control voltage as illustrated by Eq.(3). The Fig.5(b) illustrates CNFET VCO.

4. PERFORMANCE INVESTIGATION OF FINFET AND CNFET VCO

The performance of SG DG-FinFET (three terminal FinFET) and CNFET VCO circuits in weak inversion region are investigated in this section. The SG DG-FinFET VCO circuit is designed using Predictive Technology 32nm DG-FinFET model [21] and is simulated in HSPICE. CNFET CSVCO circuit is designed using 32nm CNTFET Stanford University model [17]. The values of various parameters used for simulation for the two VCO circuit in Fig.5(a) and Fig.5(b) are enumerated in Table.1 and Table.2 respectively.

The Table.3 shows the results obtained by simulating CNFET and SG DG-FinFET VCO with varying supply voltage. SG DG FinFET VCO exhibits better output frequency compared to CNFET VCO. This is by virtue of shorted gates. The shorted gates alter the threshold voltage of device. Fig.6(a) and Fig.6(b) illustrates the plot of gate to source voltage versus the drain current for N- type SG-DGFinFET, N type-IG DG FinFET and NCNFET. It is clear from Fig.6(a) that with SG configuration, threshold voltage of the device decreases and the drive current is increased which results in increase in performance of SG DG FinFET VCO. However, this increase in performance (frequency) has detrimental effect on power consumption of FinFET VCO as illustrated in Table.3. Fig.6(b) illustrates that the off current (for V_{GS}=0V, V_{DS}=supply voltage) of FinFET is increased by an order of magnitude compared to CNFET leading to further increase in power consumption.

Table.1. SG FinFET parameters and their corresponding values

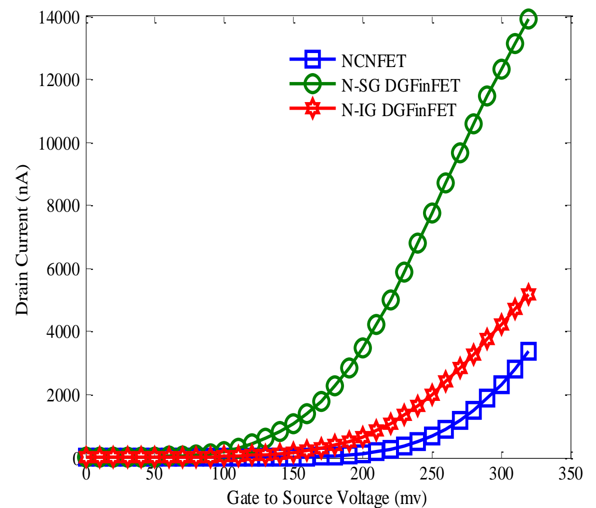
Parameters	SGN MOSFET	SGP MOSFET
Gate length	32nm	32nm
Body thickness	8 nm	8 nm
Oxide thickness	1.4nm	1.4nm
Doping Concentration of channel	$2x10^{16}$ cm^{-3}	$2x10^{16}$ cm^{-3}
Threshold Voltage	0.29V	-0.25V

Table.2. CNFET parameters

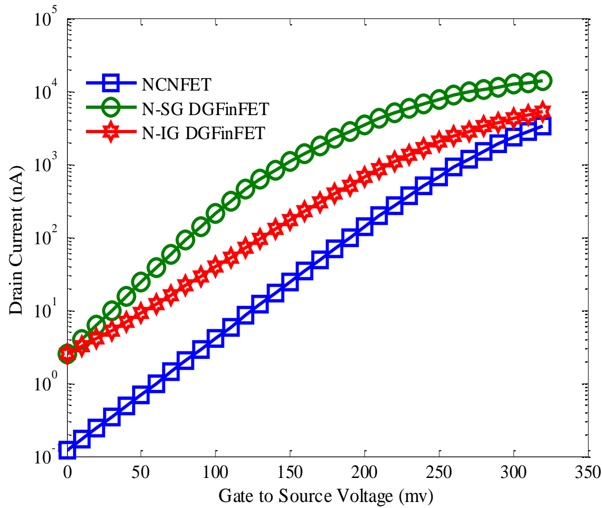
Parameter	Values
Length of Channel	32.0 nm
Doped CNT Source Side Extension Length	32.0 nm
Doped CNT Drain Side Extension Length	32.0 nm
Dielectric Constant of Gate	16.0
Oxide thickness	4.0 nm
Pitch of CNT in CNFET	20.0 nm
Chiral index	(19,0)
Total number of tubes in CNFET	3

Table.3. Performance Comparison of FinFET and CNFET CSVCO

Supply Voltage (mv)	Frequency (MHz)		Power (nW)	
	CNFET VCO	FinFET VCO	CNFET VCO	FinFET VCO
150	235	476	2.22	35.4
175	339	618	3.74	60.4
200	423	759	5.60	92.2
225	460	949	7.50	134



(a)



(b)

Fig.6. Transfer Characteristics for 32nm N type SG DGFinFET, N type-IG DGFinFET and 32nm NCNFET (a) Linear scale (b) Log scale

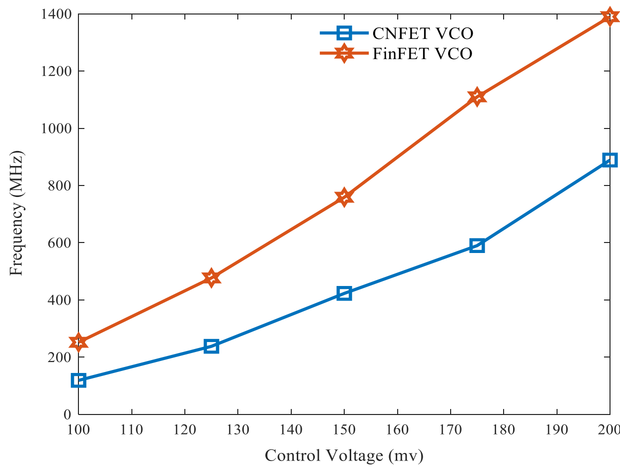


Fig.7. Frequency tuning range of FinFET and CNFET VCO

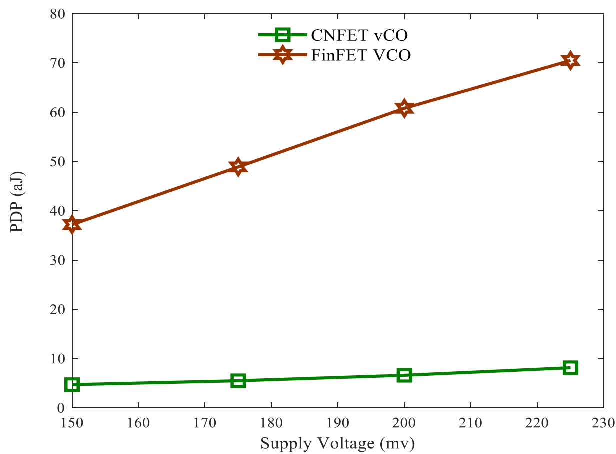


Fig.8. PDP comparison DG FinFET and CNFET CSVCO with variation in supply voltage

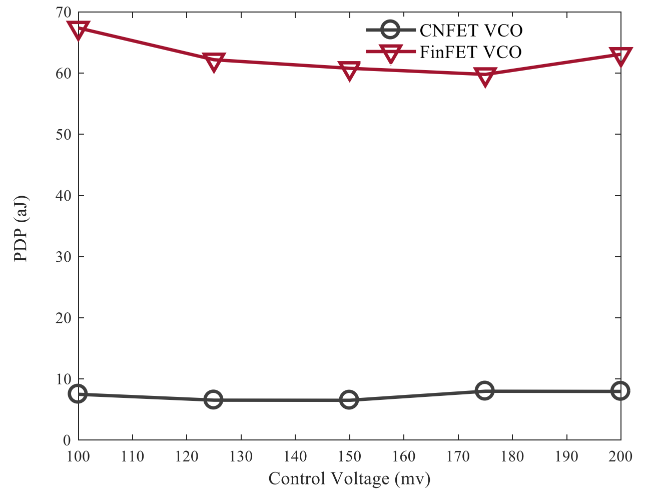


Fig.9. PDP comparison DG FinFET and CNFET CSVCO with variation in control voltage

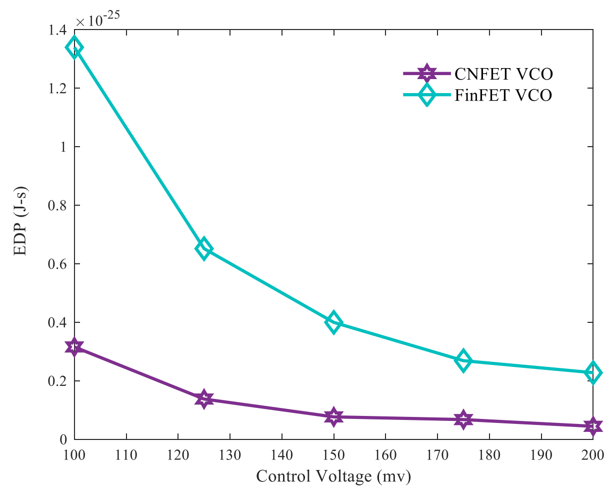


Fig.10. EDP comparison DG FinFET and CNFET CSVCO with variation in control voltage

In order to investigate the tuning range of VCO, control voltage of the two VCO circuits is varied and the corresponding frequency is observed for constant V_{DD} of 200mv. The simulation results are illustrated in Fig.7. SG DG FinFET VCO exhibits a wide tuning rang thus, indicating the superior performance compared to CNFET VCO.

Energy efficiency is a primary requirement for battery operated applications. Energy efficiency of a circuit is appropriately provided by PDP metric. PDP of SG FinFET and CNFET VCO are investigated. Fig.8 illustrates PDP of SG DG FinFET and CNFET VCO. CNFET oscillator exhibits better PDP results, showing a decrease in PDP by 89.11% for V_{DD} of 200mv, compared to DG-FinFET CSVCO and therefore CNFET VCO is more energy efficient. The variation in PDP and EDP with control voltage variation is depicted in Fig.9 and 10. CNFET CSVCO exhibits better PDP as well as EDP compared DG-FinFET CSVCO in sub-threshold regime.

VCO provides reference for switching of signals in synchronous applications. Therefore VCO stability against process parameter deviation and temperature fluctuation needs

paramount consideration along with the performance. As illustrated by Eq.(3), the output frequency of VCO is function of drive current and capacitance. The oxide thickness variation causes sub threshold slope and thereby the drive current to vary. Moreover oxide thickness variation also affects the gate capacitance. Furthermore, the heterogeneous design paradigm is incorporated in modern VLSI chips to ensure better speed and low power. The performance centric and power efficient circuits are integrated together in the modern chips. This in turn leads to large on chip temperature gradation. Also, various power management techniques employed in modern chips like applying different voltages to the devices in circuit under different circumstances contribute to increase in temperature. These temperature fluctuations cause perturbations in drive current. Therefore it becomes utmost important to investigate the thermal stability of circuits. Therefore robustness of FinFET and CNFET VCO against oxide thickness and temperature variation is investigated and the simulation results are depicted in Fig.11-13. As temperature increases the drive current in sub threshold region increases, thereby increasing the frequency for both SG DG FinFET and CNFET VCO as illustrated in Figure 11.

The oxide thickness is varied for SG DG FinFET VCO. Since front and rear oxide contributes to the gate capacitance in SG DG FinFET VCO, this VCO shows larger variation in frequency for oxide thickness variation compared to CNFET VCO.

The parasitic capacitance dominate the intrinsic capacitance if oxide thickness is very thin in sub threshold DG FinFET leading to increase in off current and circuit delay [22]. Therefore, the PDP of FinFET circuit shows more variation with oxide thickness variation compared to CNFET VCO as illustrated in Fig.12. Also, SG DG FinFET VCO exhibit 15% more variation in PDP compared to CNFET VCO with variation in temperature for nominal oxide thickness. This is because of improved thermal stability of CNT in CNNFET. Moreover, DG FinFET shows higher variation in EDP compared to CNFET VCO with variation in oxide thickness as illustrated in Fig.13.

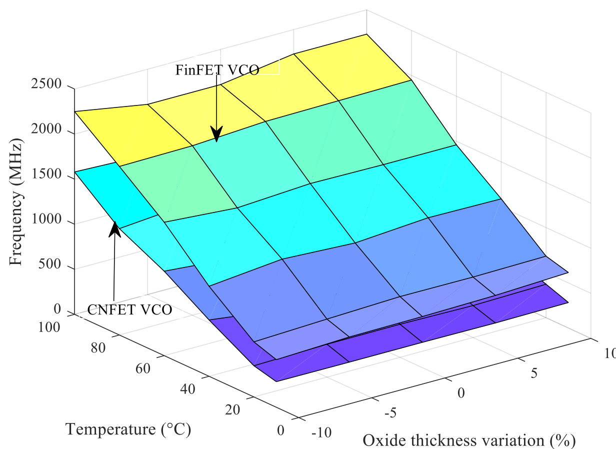


Fig.11. Variation in frequency with temperature and T_{ox}

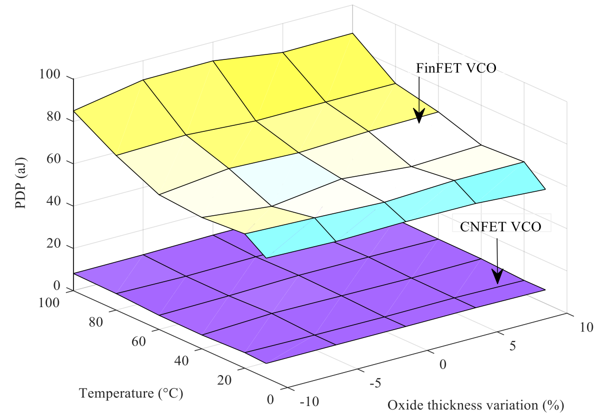


Fig.12. PDP variation with temperature and T_{ox}

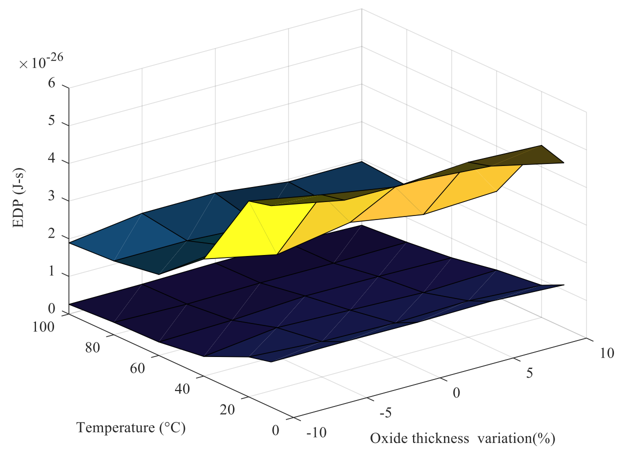


Fig.13. EDP variation with temperature and T_{ox}

5. CONCLUSION

Performance comparison of DG-FinFET and CNFET based CSVCO in sub-threshold regime is accentuated in this work. The performance analysis results show that SG DG FinFET VCO exhibits better output frequency and tuning range compared to CNFET VCO. However, SG DG FinFET VCO exhibits higher power consumption compared to CNFET VCO. Furthermore, the energy efficiency investigation of VCO indicate that CNFET VCO is more energy efficient compared to DG FinFET VCO. Also the variability analysis indicates that CNFET VCO exhibit better immunity to the oxide thickness and temperature alterations compared to FinFET VCO. Thus, CNFET VCO exhibit better performance in terms of PDP, EDP and robustness compares to FinFET VCO and therefore proves to be a viable choice for sub threshold region.

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