BASIC SIGNAL PROCESSING SYSTEM DESIGN ON FPGA USING LMS BASED ADAPTIVE FILTER

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Vaibhav Kadam[1], R. G. Dabhade[2], A.B. Gaikwad[3]

[1,2,3]*Department of Electronics & Telecommunication Engineering, SND COE & RC Yeola, M.S, INDIA.*
vaibhavskadam15@gmail.com

Abstract

Adaptive digital filter based on LMS algorithms widely used in the area of digital signal processing to iteratively estimate the statistics of an unknown signal. Design of an adaptive filter is based on three major computing elements namely multiplier, adder and delay unit torealize the Finite Impulse Response (FIR) filter. The filter weights(coefficient) of the FIR filter are adjusted automatically by Least Mean Square of the error so as to match the adapted output to the desired input. This paper explains the design of adaptive filter by two approaches. One is model based approach and other is Field Programmable Gate Arrays (FPGAs). The model based design approach is developed around MATLAB, SIMULINK and SYSTEM GENERATOR tools, which provide a virtual FPGA platform. Modern FPGA include the resources needed to design efficient filtering structures. The LMS algorithm has been implemented on CYCLONE II EP2C35F672C8 FPGA device, using ALTERA QUARTUS II development platform. The three major demonstrable applications cited in the present work are System Identification, Noise reduction and Echo cancellation.

Keywords – *Signal Processing; FPGA; Adaptive Filter; DE2KIT*

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I. INTRODUCTION

Embedded Systems Design is an interdisciplinary subject, dealing with issues ranging from hardware, software, tool, algorithm and domain. The vast domain of electronics systems can be classified into three major section namely, Control, Communication and Computing.The objective is to understand Computing methodologies and technologies from system design perspectives in a structured approach i.e. identify, study and practice platform specific tools to design, debug, and optimize electronic systems and concluding the study by implementing a project with prototype model for final demonstration.

The DSP applications enforce many constraints on size, speed, cost and power dissipation. Thus it is necessary to choose the designing tools very carefully. The very popular tools used for such design of applications are FPGA, DSP and ASIC. The DSP gives a mathematical analysis of system but have some limitations. Due to the serial architecture of it, it cannot process on high sampling rate applications.

Whereas ASIC used for dedicated applications so it have less flexibility and require long design cycle. The FPGA overcomes the limitations of DSP and ASIC. Thus FPGA becomes very popular platform for designing of signal processing applications due to their flexibility and parallel architecture.

This paper explore the area of both Model based, FPGA based approaches and combination of both as Hardware in the Loop (HIL) for adaptive filter design.

In model based, MATLAB/Simulink/ System Generator environment is used. Synthetic signal generation using equation based dynamic function and simulink blocks facilitate the experimentation in Lab environment.

In FPGA based approach the audio signal chain is established as the first step and then the Adaptive FIR filter processing block is inserted in the chain. The hardware setup is shown in Figure-1, which include Altera FPGA DE2 KIT, signal generator, DSO, Altera Quartus IDE tool for HDL code compilation on computer and finally downloading the code by JTAG cable on to FPGA Kit.

The paper is organized as; section II describes the audio signal chain establishment. Section III describes the Model based signal processing. The FPGA based signal processing is covered in section-IV. Conclusion and references are the concluding sections.

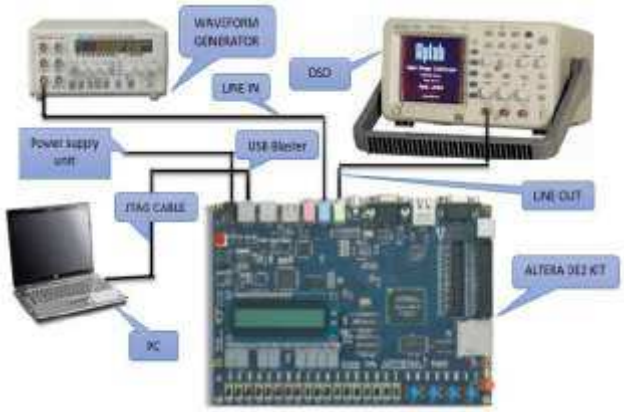

Figure-1 Signal Processing Hardware Setup using DE2KIT.

II. SIGNAL CHAIN ESTABLISHMENT

Signal chain establishment [1] is the first step in the design process of signal processing on FPGA. The analog audio signal generation, digitization using ADC section of an audio codec, Serial to parallel (SIPO) , Parallel to serial (PISO), and converting back to analog signal using DAC section of audio codec are the modules of the audio signal chain as shown in Figure-2.

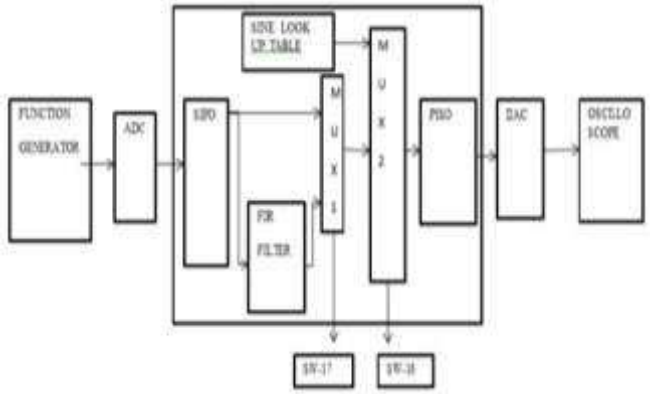

Figure 2. Establishing signal chain

Signal Generation can be by three methods; signal generator equipment, digital signal synthesis in FPGA and MATLAB based signal generation. Signal generators are available from a host of vendors in all price range. Digital signal synthesis in side FPGA logic is very useful for HDL data path simulation and testing. Sine waveform can be generated using simple look up table in FPGA. Numerically controlled Oscillator (NCO) IP cores in FPGA can be used to synthesize complex waveforms. MATLAB is an efficient modelling tool for source signal generation, processing using various algorithms and signal analysis using virtual sink sources like oscilloscope, spectrum analyzer, etc. In case of filter design audio signal generation can be by playing audio files in various formats as shown in green block in Figure 3 and Figure 5. In Adaptive filter design, two signal sources are required; one for the unknown X[k] and the other for the desired D[k]. It's very handy to generate these stereo signals using MATLAB and deliver them through headphone connector of the computer as shown in blue block in Figure 3 and Figure 5.

Artificial synthetic ECG signals shown in Figure -4 can be generated by Dynamic function. Such functions are usually equation based [5]. Echo generation using MATLAB simulink model [2] as shown in Figure-5.

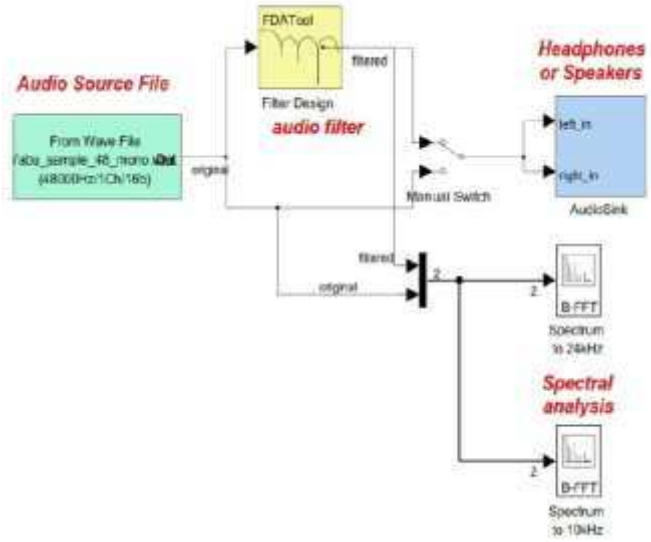

Figure-3 Simulink Models for FIR filter design.

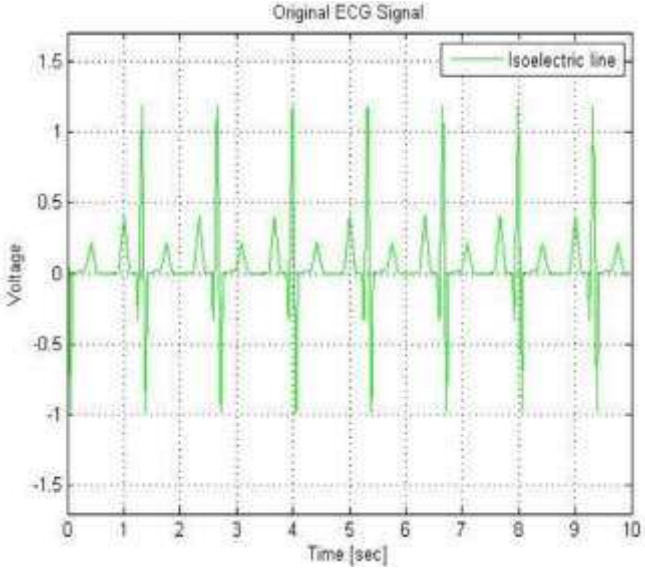

Figure-4 Dynamic function based synthetic ECG signal

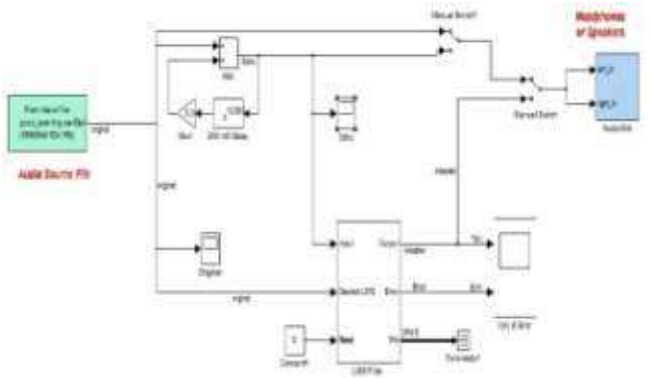

Figure-5 Simulink Model for Echo generation

III. SIGNAL PROCESSINGMODEL

The best approach for designing of an embedded system is model based approach. There are so many tools are available, which gives facilityof easy to design of hardware & software before actualimplementation of the system.

Model based design helps to design, simulation and code generation for any one of Processor/Microcontroller,DSP and FPGA platforms. In this work we have been used MATLAB, SIMULINK tool from Math-works and system generator tool from Xilinx.

System Generator is a system-level modeling tool that provide the facility of FPGA hardware design. The Simulink provide well suited modeling environment for hardware design. This gives high-level abstractions that are automatically compiled into an FPGA quickly. The system generator tool can be used to generate target specific, accurate, synthesizable Verilog and VHDL code.

System Generator based single order LMS algorithm module is replicated for all the three applications; System Identification, Echo cancellation and Noise reduction as shown in Figure 6, 7, 8. The step size of the LMS algorithm is variable and can be adjusted to minimize the error E[k] and to get more accurate output Y[k]. The System Generator Wave Scope block used in the model gives easy-to-use waveform for analyzing and debugging. Here it allows observing the time-changing analog values of the adapted coefficient of the single order LMS after the conclusion of the simulation.

Figure-6 shows the system generator based of system identification design [3]. In this system, the green color module at the top in figure-6 is unknown system which is to be identified by the LMSalgorithmmodules. The unknown system is asingle order Finite Impulse Response (FIR) filter which basically reduces the gain ofthe input signal.

Figure-7 shows the system generator based of noise cancellation design. The signal and the noise are generated separately and then combined by an analog summer. This mixed signal is the unknown signal X(k) and the noise is the desired signal D(k). The noise free original signal is retrieve by subtracting adapted signal Y(k) from unknown signal X(k).

Figure-8 shows the system generator model of adaptive echo cancellation design [2]. Here the mux1 is used to generate the echo by adding the sine signal and the sine half signal. Mux2 is used to pass the desired signal.

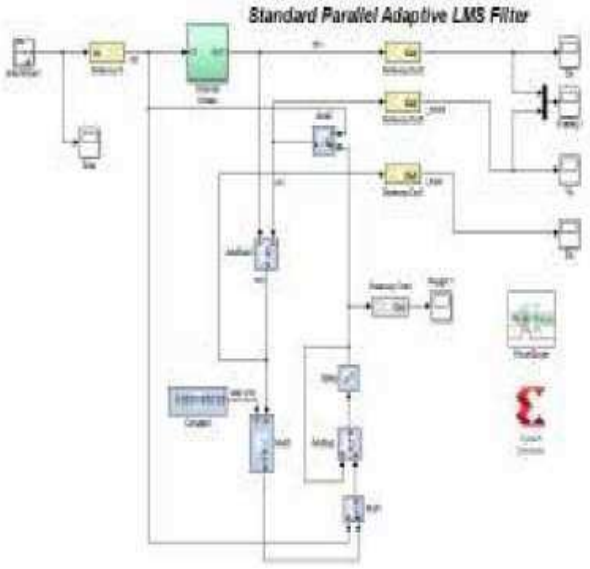

Figure-6 System Generator based system identification

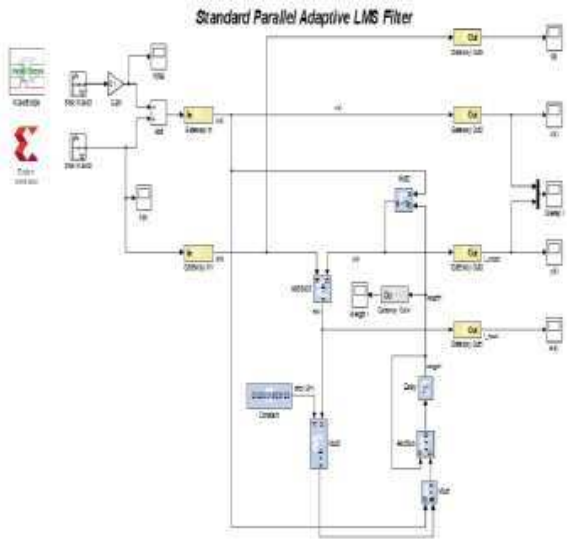

Figure-7 System Generator based Noise cancellation

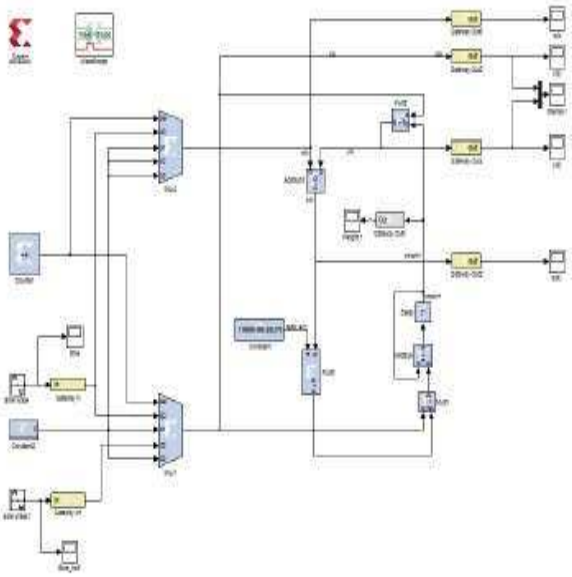

Figure-8 System Generator based Echo cancellation

IV. FPGA BASED SIGNAL PROCESSING

The data path architecture for LMS adaptive filter in FPGA is shown in Figure 8. In this workwe used board 50 MHz clock to generate 100 KHz I^2C (Inter Integrated Circuit) clock. In this work generate a master clock of 18.4 MHz Audio_CK from the 27 MHz clock of external codec for I^2S interface for audio codec. This master clock is used to operate audio left-right clk at 48 KHz as we as audio bit clock at 1.536MHz.

Covert the external signal into digital form and this is done by Analog to Digital Converter section of the stereo audio codec which is given to FPGA. This digitized signal is provided at bit clock rate in the form of Audio_ADC_LRCLK clock and Audio_ADC_Data signal. Simultaneously the 16 but serial audio ADC datais converted into parallel form using SIPO module. This parallel data is given to MUX-1and MUX-1 used this data

to selection of either internal or external noise mixed signal in FPGA. The adaptive filter module have 4 output signals such as X(k), D(k), Y(k) and E(k). This four signals are used by MUX-2 for switching operation. The output of MUX-3 is either adapted output signal or external data signal. MUX-4 receives the input from the output of MUX-3. The MUX-4 is used to select the either the internal pure sine wave or adapted output signal. The output of MUX-4 is converted into serial from using parallel in serial out (PISO). This serial output signal is applied todigital to analog converter block of audio codec. Finally these signals are observed on oscilloscope.

DE2 board have a several number of switches, out of these we are used as to select inputs of various multiplexers as shown in Figure-9.

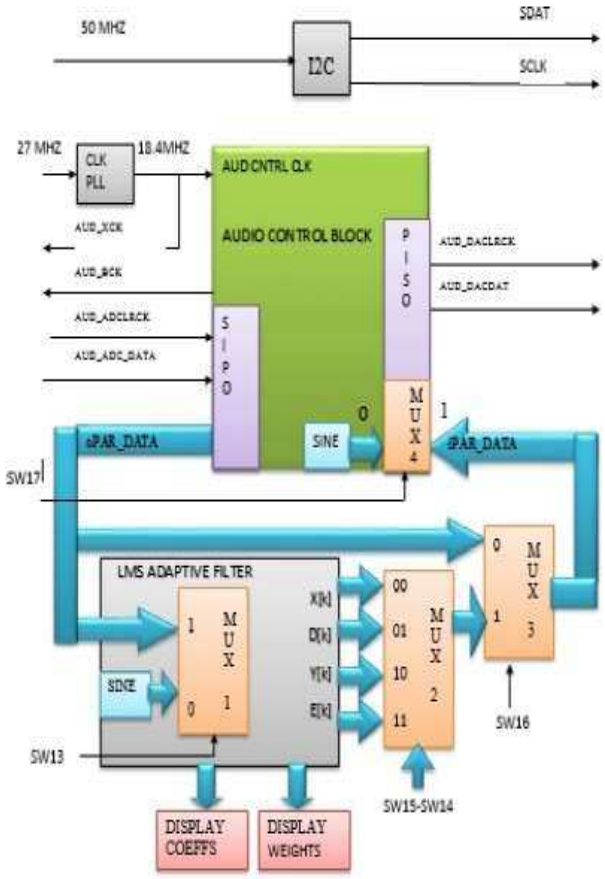

Figure 9 Data path architecture of LMS adaptive filter in FPGA.

Switches assigned as follows:

Table I

SWITCH	OFF (0)	ON (1)
	Signal	Signal
13	External	Internal
17	Internal	External
16	Internal	Adapted

Table II

SW 15	SW 14	SINGLE CHANNEL	MULTI CHANNEL	
		SIGNAL	LEFT CHANNEL SIGNAL	RIGHT CHANNEL SIGNAL
0	0	X(K)	X(K)	D(K)
0	1	D(K)	Y(K)	E(K)
1	0	Y(K)	X(K)	Y(K)
1	1	E(K)	D(K)	Y(K)

V. CONCLUSION

Present work envisages, signal generation and algorithm based signal processing using Model based approach and suitable data path architecture on FPGA platform. The LMS algorithm has been implemented on CYCLONE II EP2C35F672C8 FPGA device, using ALTERA QUARTUS II development platform. The complete FPGA design cycle of HDL Coding, Simulation, Synthesis, Implementation and Testing on FPGA Target system is practiced through the ADAPTIVE filter implementation. The three major demonstrable applications cited in the present work are System Identification, Noise reduction and Echo cancellation.

REFERENCES

[1] SashankShekharPujari, PrangyaParamitaMuduli, AmrutaPanda,RasmitaBadhai,SofiaNayak, YougajyotySahoo, Design & Implementation of FIR Filters using On-Board ADC-DAC & FPGA, International Conference on Information Communication & Embedded Systems (ICICES 2014)

[2] SashankShekharPujari, Amruta Panda, P K Dash, Design &Implementation of FPGA based Adaptive Filter for Echo Cancellation, International Conference on Convergence of Technology - 2014

[3] P.K. Dash, SashankShekharPujari, Er.YougajyotySahoo, Design and Implementation of Single Order LMS based Adaptive System Identification on Altera Based Cyclone-II FPGA, International Conference on Communication and Signal Processing, Tamilndau, India, April, 2014 (ICCSP14).

[4] Patrick E. McSharry_, Gari D. Clifford, Lionel Tarassenko, and Leonard A. Smith, A Dynamical Model for Generating Synthetic Electrocardiogram Signals, IEEE Transactions on Biomedical engineering, Vol. 50, No. 3, March 2003.